Status report on the Schmidt telescope CCD camera controller.

Alain Maury - February 1994

This document describes the design of a new CCD camera controller adapted to Schmidt telescopes.

It contains the following sections :

Generalities
Choice of the detectors
Implementation of a multi CCD camera
Controller boards design requirements
Controller design
Electronic components selection
Current status
Test system
Future readout system
Performance of a 9 wide CCD camera in sky surveillance

the schematics of the controller can be found in appendix 1, and the data sheets of all the major components in appendix 2

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12. ABSTRACT (Maximum 200 words)

This document describes a new CCD camera controller adapted to Schmidt telescopes.

This report contains the following sections:
Generalities; Implementation of a multi CCD camera; Controller boards design requirements; Controller design; Electronic components selection; Current status; Test system; Future readout system; Peformance of a 9 wide CCD camera in sky surveillance; plus
Appendix 1 Schematics of the controller
Appendix 2: Data sheets of the all the major components

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Generalities

A typical "big Schmidt" telescope focal plane is in the order of 30 to 35 cm wide, with a focal lentgh not too different from 3.15 meters, giving a scale of 1 arc minute per mm, or 15 microns per arc seconds. Because of optics, the focal locus is a sphere, and this requires to bend the photographic plates in use, or to use field flattening elements in front of flat detectors, unless they intercept a part of the sphere small enough to be considered flat (typically less than 10 mm wide).

The very small size of CCD detectors has prevented their use inside Schmidt telescope until now when technology and reduced price allowed to design multi CCD cameras. On the other side, many photographic plates have been discotinued by Eastman Kodak, and replacement technology, even if less efficient have to be developed. It is already impossible to make "V" photometry using currently available photographic plates.

Because these telescopes are usually not "hot new" telescopes, and because of the high price of the technology used, it is important to find ways to dramatically lower the price of these cameras so as to be able to convert from photography to CCDs. For example, a typical price for a thinned 2048*2048 pixel chip from Tektronix is in the order of $80,000 a piece. A detector which would require 8 such chips would already cost $0.64 millions. A "normal" price for a camera and its controller without CCD is in the order of $15,000 a piece. The complete price of such a camera could easily cost several years of operating budget for these instruments using existing technology. It is therefore necessary to rethink this problem in the light of low costs off the shelf CCD chips, and very compact camera electronics. Usual cameras are mounted at the back of the telescope, and can be quite large without any particular problems. A typical plate holder is only 5 to 10 centimeters thick, and being in the optical path cannot generate much heat without affecting the quality of the images. A final aspect of this design is that the controller have to be much faster than the typical astronomical CCD controller. The reasons for this are discussed below.

Covering as much field as possible using this type of focal plane requires using either relatively large individual CCDs or a larger number of smaller one. Because this approach obliges to use a large number of individual CCDs or multiplex the data, it is either an expensive one or a slower one.

Price considerations led to the use of off the shelf CCDs. In fact grade 4 CCDs are used. They usually have a relatively high number of cosmetic defects, but most of these are hot spots (pixels generating a very high thermal signal), and when the CCD is cooled down (lower than -30° C), these hot pixels dissapears, and the CCD becomes almost as good as a grade 1 CCD, with only a few defects such as dead lines and the like. However, the price difference is such that 9 grade 4 CCDs are less expensive than a single grade 1 device (in fact the production of these

CCDs have made such progresses that most of the chips sold as grade 4 are in fact grade 3 or better).

- It could have been possible to put all the CCDs in a single dewar, but the fact that the CCDs must be aligned very precisely tangential to the focal plane, plus the fact that a field flattening lens must be used led us to choose a different approach. If a single field flattening lens is used for all the CCDs, it will be large, thick, expensive and moreover will have poor optical quality (chromatic aberration). By using individual compact modules, each CCD is covered by a single thin plano convex lens. CCD alignement will be performed using a series of sky tests which will provide for each module information on focus, alignement and tilt on the optical axis.

To resume this section, a CCD controller adapted to Schmidt telescope ought to be :

- Compact (6*9 cm board in this design)
- Cool (no heat generation in the optical path)
- Fast (200,000 pixels per seconds)
- Inexpensive
- Self contained, so as to lead to multi CCD modules cameras
- Fiber optics based so as to avoid cross talk between modules

Choice of the detectors

The approach chosen here is to use relatively large CCDs (i.e. 2048*2048 pixels), and design a very compact electronic controller which is closely coupled with its camera. In fact, we are able to build most of the camera controller into a board which is merely 55*90 mm long. A power supply and bias voltage board is outside the telescope and connect to this main board via a flat ribbon cable. 5 fiber optics allow data exchange between the readout system and the controller (line start, master clock, A/D clock out, A/D output 1, A/D output 2). The use of fiber optics guarantees minimal crosstalk between individual camera modules.

After much searching and discussions, 2 vendors of inexpensive and large CCDs were selected. From both of them we were able to obtain prices in the order of $2,000 to $2,500 per grade 4 device, their data sheet is in this report. Their main characteristics are listed below :

Brand name	Loral	Kodak
Size	2048*2048	2048*3072
Pixel size	15 microns	9 microns
Physical size	31.72 mm	18.43 *27.65 mm
Angular field of view	34.5 '	20 *30'
Number of CCDs/5 degrees	9	10
Pixel scale	0.979 "	0.587"
Readout registers	2	2
Full well potential	120,000 e-	85,000 e-

We finally chose to use Loral CCDs because they presented several interesting features. Their larger size allowed to implement the positioning scheme described below, the pixels larger size was not felt to be a problem in normal seeing conditions at our observatory. Finally, it is possible ot use them in a partially inverted mode which doubles the dynamic range (to 220,000 e-) while supressing the blooming around bright stars. This didn't seem possible using the two phases of Kodak CCDs, eventhough their smaller pixel size would have allowed a better sampling of the images (at the cost of an even larger number of data to reduce).

These Loral CCDs are produced in Milpitas (CA - USA) and are different from the scientific Loral chips produced in Newport Beach (CA - USA). The orientation of the Milpitas plant is toward commercial devices (infact our chip's main commercial use is for Hasselblad's camera CCD backs), the production plant is more "industrial" than the Newport beach plants, and the yield of good chips is said to be much higher there. These CCDs are thick front side illuminated chips, which do not have a good blue sensitivity, but overall provide a quantum leap compared to photography since a 2 minutes exposures detect stars which would have required more than 30 minutes of exposures using a photographic plate. On the other hand the blue sensitivity is so poor that a IIaO plate does seem to give better results in the B band. In V the camera perform already much better than plates, and in red and infrared, the "speed" (as judged visually on the processed frames) is much better (5 to 10 times) than photographic plates. In Z band (1 micron band), the CCD sensitivity is not very high, but several 100 of times better than the 1Z plates, leading to potentially interesting results during the full moon, where Schmidt telescopes are normally unused.

Implementation of a multi CCD camera

The following diagram gives a rough idea of the mechanical implementation of each camera module and their installation inside a plate holder.

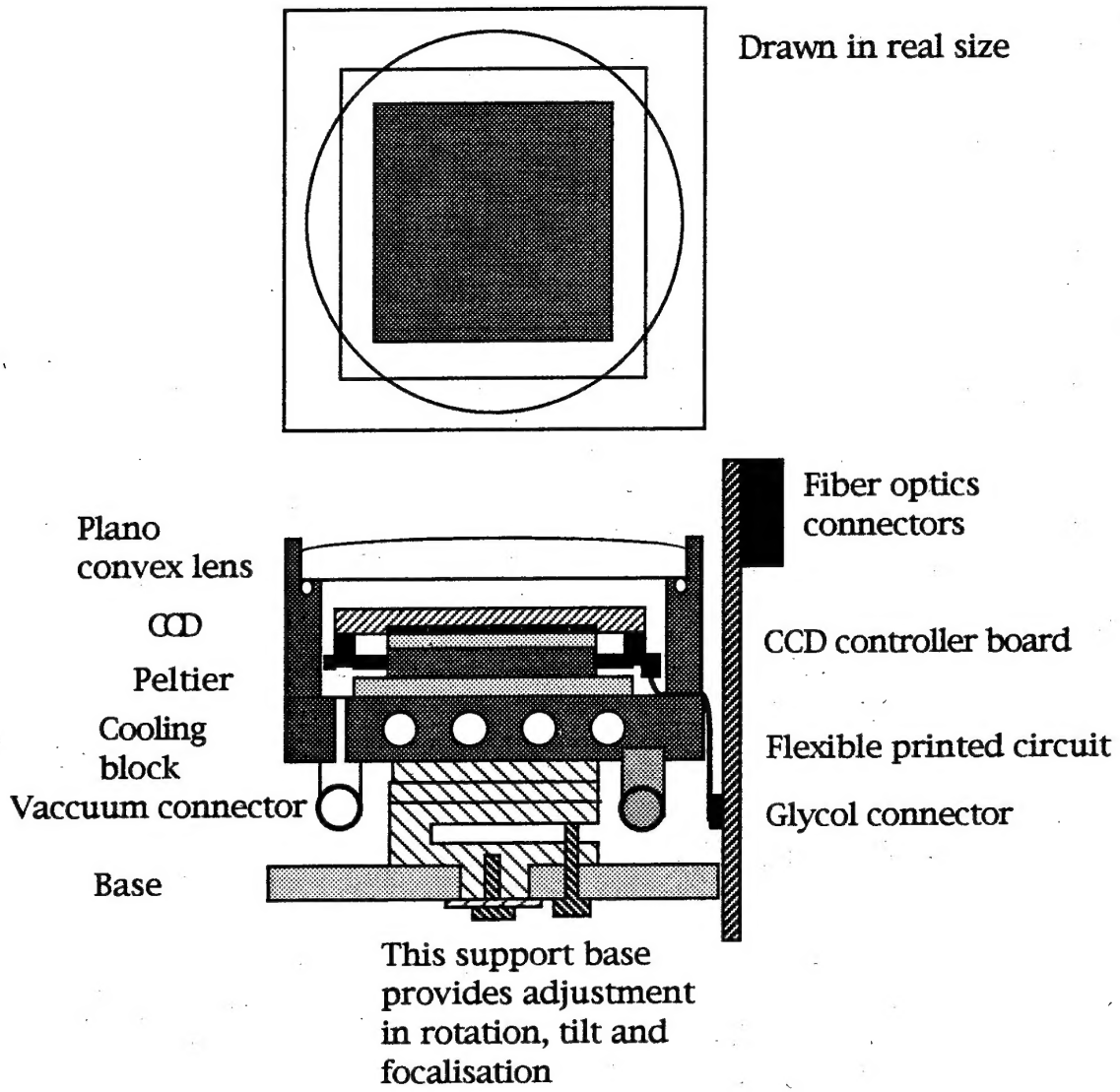
There is only a very slight overlap between each CCD (more precisely the distance between two sensitive surface is slightly less than the size of a single CCD's surface).

Several modes of observing are available with this positioning of the individual CCDs, 2 are described in the previous page.

The RA shift mode will likely be the "normal" mode of the camera, eventhough a scan mode will also be available. A version of the quad exposure mode will use "shift and add" technique to allow deep exposures to be made. While a filter wheel is currently used with our mono CCD camera system, only two filters will be available in unnatended mode with this camera (i.e. without having to bring the

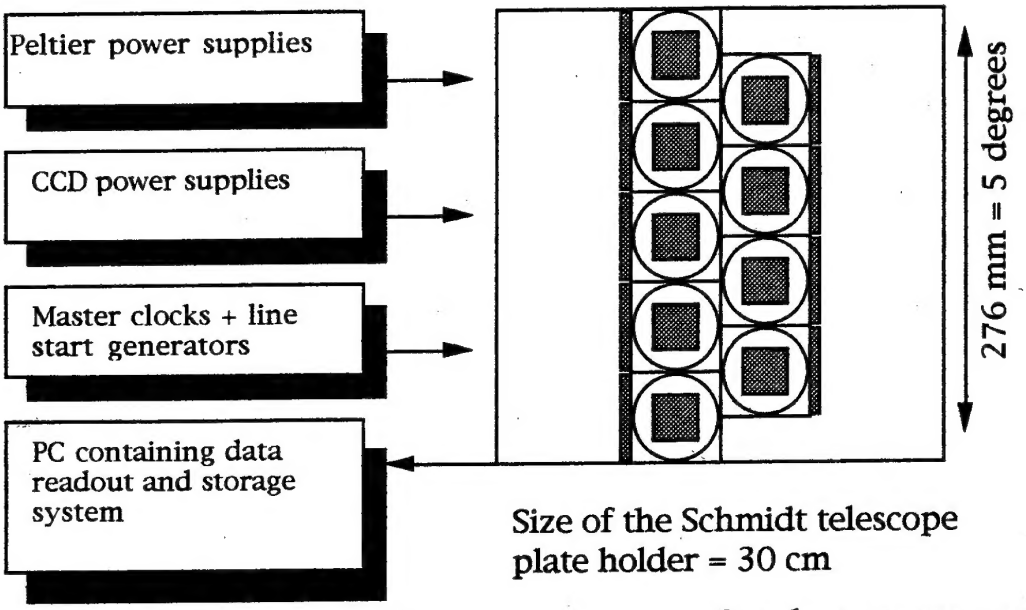
telescope down and reload a new filter set). These filters units will contain 9 individual 50mm square filters on a single plate.

Individual CCD modules - Simplified plans - October 1993



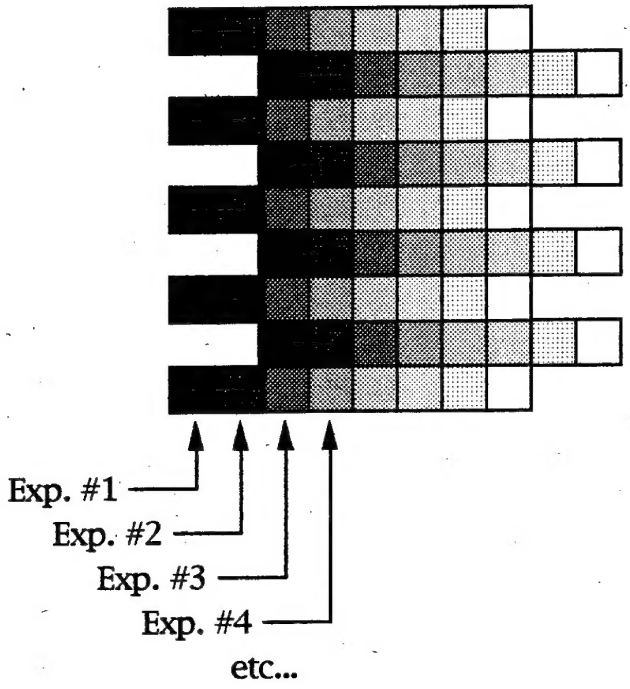
The positioning of the individual modules is similar to the way a horse moves in a chess game. The CCDs are organised in 2 rows (4 others could be put inside the telescope plate holder).

Positioning of 9 CCD modules in the focal plane of the Schmidt telescope

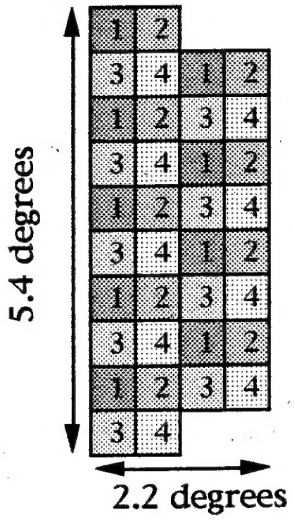


Size of the Schmidt telescope plate holder = 30 cm

RA shift mode : Several exposures with a 30 arc minutes drift in right ascension give several overlapping images of the sky.



Quad-exposure mode : 4 individual exposures recreate a contiguous 11 square degrees exposure



Controller boards design requirements :

- The first requirement was space. The controller had to be as small as possible, and because each camera had to be roughly 6 centimeters from the next one, one of the physical dimension of the board had to be smaller than this. It was chosen to use surface mounted components for this reason (SOIC packages). At first, we thought we would have to build two boards (one for the logic signals, another for the analogic parts, both boards being mounted on a common mother board), but then realised that it was possible to fit all the components on boht sides of a single board. On the other hand, the power generation boards can be any size, and for practical reason, we chose to implement them on euroboard format cards (100*160 mm).
- The second requirement was acquisition speed. While it is a known fact that the readout noise grows as the square root of the readout speed, a small model convinced us that because of the high photon flux provided by our telescope it was a better use to have a fast readout controller so as to collect light as often as possible. The relative aperture is F/3.5, and for an exposure without filter, we find a typical photon flux of 150 photons per pixel per second (depending on wether or not the mooon is in the sky, less than 150 if the sky is dark, and up to 5 times that value during the full moon). The detection of faint stars will depend of the precision at which we can measure the sky background. If we compare with the current controller which has a 110 seconds readout time, with 19 electrons readout noise, not taking thermal noise into account (1 e-/sec.) , we can compare two situations where the acquisition of a single image (exposure + readout time) will be done in 4 minutes :

Slow readout : 130 seconds of exposure, 110 seconds of readout time (38130 pixels/seconds).

During a 130 seconds, the photon flux per pixel is 19500 electrons, with a photon noise of 139.64 e-. The quadratic sum of 19 e- (readout noise) plus 139.64 e- (photon noise) is 141 e-. The photometric precision on the sky is thus 0.72%

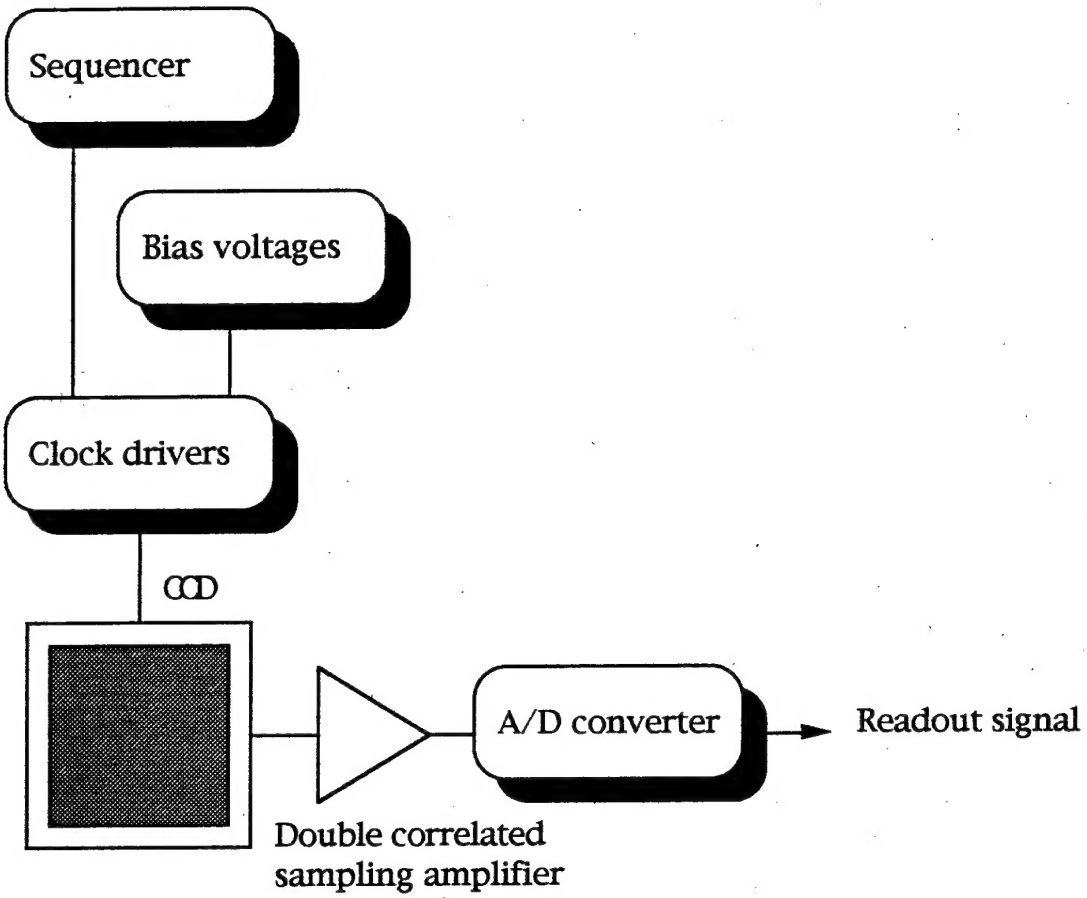
Fast readout : 230 seconds of exposure, 10 seconds of readout time (using both CCD amplifiers, or a readout rate of 2x200,000 pixels/seconds, or 5.5 times faster than in the preceding example).

In this case, the photon flux is 34500 photons with a noise of 185.7 e-. The readout noise should be 2.34 times higher (square root of 5.5) at 44.58 e-. The quadratic sum is 191 e-, and the final precision at which one can measure the sky level is 0.55%, or a 30% increase compared to the slow readout mode. Compared to other applications, it is clear that a faster readout rate is better adapted to Schmidt telescopes.

Controller design

Generalities :

The typical organisation of an astronomical CCD camera is the following :



The transfert of charges inside the CCD is done with periodic signals (referred to as "clocks"), which have peculiar patterns and voltages (such as 1.5 volts to - 8 volts for examples).
These clocks are generated inside a sequencer which usually uses TTL signal levels (0 to 5 volts), while the voltages used for the clocks as well as for certain bias voltages used by the CCD amplifier stage are generated inside a bias voltage generation system. It is the role of the clocks drivers or "level shifters" to change the TTL clock levels to the voltage levels required by the CCD, as well as to amplify these signal to drive the CCD. Provided everything is correct with the clocks patterns and voltage values, the CCD generates a video signal during its readout. This signal is amplified using a double correlated sampling amplifier which extracts out of the peculiar video signal generated by the CCD values which is then fed to an analog to digital converter. This sends then data to a readout system, usually located relatively far from the telescope.

Electronic components selection :

- Finding the right parts to use in this controller has been a long process, and the final design of the main controller board is quite new compared to existing models. It is very optimised for its purpose.

- The voltage generation board does not contain any "clocking" signals. On the other hand, it generates heat, and is better located outside the telescope tube. We used a very classical design which uses a voltage reference, with source followers adjustable through multi turn trimmers. Other classical voltage sources (+/- 5 volts, +/- 15 volts) are generated using classical regulators. This board is connected to the main controller's board by a flat ribbon cable.

- The main controller board has to be very compact (5.5*9 cm at most). The smaller the number of connectors required, the higher the reliability of the camera. All the parts had to be available in SOIC package (surface mount). The only exception to this are the fiber optics connectors.
- To avoid crosstalk between the different camera modules, all oscillating signals have to be brought in and out using fiber optics. Because most fiber optics drivers are not directly TTL compatible, they require separate circuitry. After some search effort we located Toshiba parts which were fast enough for our purpose and directly TTL compatible (TOTX194 and TORX195). These parts alone cost almost one third of the components cost of this board.
- In order to operate several CCDs in a relatively small space either synchronously or asynchronously, it was necessary to have a single sequencer per module. After very long delays searching for the right part, we finally located Intel's new flexlogic IFX780 EPLD. This device contains 8 blocks which can be configured as either RAM or EPLD. Its development system can be purchased at low cost (which is not the case of the Altera part that we meant to use at first which costs around $12,000 alone). In our application, some of the modules are programmed as a sequencer for the RAM, and the RAM part contains all the clocking pattern required to operate the CCD. In anti blooming integration mode, it is possible to drive one part of the IFX780 using a slower clock rate (self generated from the master clock by a frequency divider in an EPLD block).
Once an IFX780 has been programmed, it can be reprogrammed on the fly using a JTAG interface (for a different clocking pattern for example). A prototype board has been built using such a device, and it is been currently programmed to perform the required task. The schematics of connection of the IFX780 attached to this report will maybe have to be redrawn in the final version of the camera following the current tests.
- We chose to use Maxim DG333A quad SPDT analog switches as clock drivers. They were the only quad drivers available in SOIC packaging. They have fast switching time as well as low Ron impedance.
- All signals going to the CCD have an adequately chosen RC filter installed near the CCD.
- In order to use both CCD amplifiers, it was necessary to have a double acquisition chain

- Because of the fast readout speed compared to normal cameras, a video clamping amplifier was chosen. Using two operationnal amplifiers, it is possible to obtain voltage gains as high as 100. Burr Brown's OPA627 and 637 are used in our design.
- To supress the DC signal provided by the CCD amplifiers, an input clamp was also added.
- To provide the four clamps required (two inputs, two for the level substraction) we chose a DG445 quad SPST analog switch. It has relatively low Ron, and very low charge injection characteristics (5 pC).
- A double A/D converter with serial outputs was required. Conversion faster than 5 microseconds was also required. Preferably an input stage sample and hold amplifier as well as internal reference voltage source was required. This plus the SOIC package and the low cost of the unit left us with the choice of the Burr Brown PCM1750, which is a double 18 bits (linear to 14 bits) 4.5 microseconds converter.
- A separate master clock board has been built. It is simply a quartz oscillator, TTL drivers so as to provide drive capability for 9 fiber optics transmitters.
- Another board has been built for the synchronous generation of line start signals. It receives a line start signal from a PC (will may be generated by a DSP in the final version), and has similar TTL drivers to drive 9 fiber optics transmitters. Both cards are installed inside the G64 rack which will also contain the bias boards.
- The Peltier elements power supply is current regulated. It is made with a simple low cost circuit using off the shelf regulators.
Because it generates a lot of electrical power (18 sources of 2 to 2.5 amps), this rack is located inside the machine room of the telescope.

Current status :

A camera using a Loral 2048*2048 CCD has been in use at our telescope since September 1993, but very poor weather has limited the number of nights used for real sky tests. Nevertheless, after 10 nights of observations (the telescope is mainly used for on going photographic programs) around 2 gigabytes of data have already been acquired with this system providing us with a sufficient amount of experience in data acquisition and reduction, as well as a large number of test images. This allowed us to better refine the use of the CCD, and among other showed very clearly that the anti blooming mode was a necessity in our application.
As far as the new controller is concerned, we discussed about the design choices with several CCD experts, among which F.H. Harris (U.S.N.O. Flagstaff) who have helped us to optimise some points in the design (choice of the analog switches for example).
After this design stage, electronic components are being procured, and construction of a first prototype of bias board and controllers will be

built. As soon as the programmation of the IFX780 is finished, sky tests will be performed using this new design.
A mechanical prototype is also being constructed. Vendors for vacuum connectors as well as connectors for glycol circulation have been located. These two systems will consist of a main connection system and distribution to every individual CCD module through a manifold.

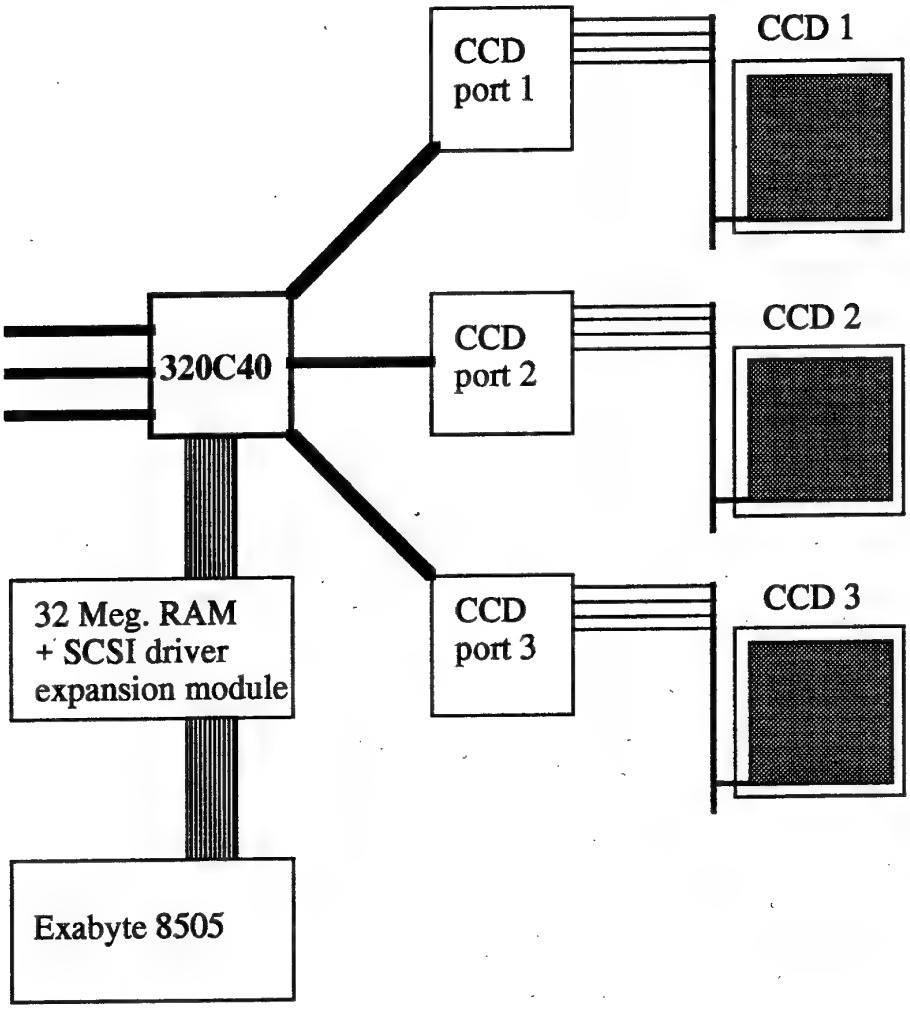
Test system :
To test the first camera using this controller, we will use a 320C30 DSP module currently in use with the existing camera. Because it relies on the PC for data storage, it will be limited in readout speed. However, it will use the controller at its nominal speed of 200000 pixels per second. There will be a delay between each line so as to allow the PC to read the data and store it on the Exabyte tape drive. Some funding has already been found so as to buy a 320C40 DSP development system and it will be put into operation as soon as possible. As soon as we get one 320C40 working, we can put three modules into operation. A new collaboration is in progress with the "Planet Erkundung"group of the DLR (Deutsche Luft and Raum Fahrt), so as to continue work on the DSP based readout system.

Future readout system :
The readout system which is envisioned is based on 320C40 Parallel Digital Signal Processors (PDSPs) which control 3 CCD cameras each. These PDSPs have a high speed 8 bit parallel port (20 megabytes per seconds). A specially designed CCD port allows the conversion of data coming from a camera (i.e. 2 outputs from fiber optics in serial form) into one of the high speed links of the PDSP. It was possible to find a vendor that would add a memory extension to his PDSP modules, as well as develop a SCSI interface for raw data storage. A typical performance of this system will be to readout three CCD images into RAM in less than 10 seconds, and then transfert the images onto Exabyte tapes in 50 seconds during the following exposure. If the exposure is longer than 50 seconds, then some amount of image processing can be performed. Otherwise the normal operating mode will be to reload the images the following day and process them so as to extract the position and magnitudes of the stars.
In the end the system will consist of a massively parallel processor so as to perform real time star detection, as well as trailed objects detection. The processing power of such a system will have to be higher than several gigaflops.

Performance of a 9 wide CCD camera in sky surveillance :
This mode refers to a mode where the widest possible angular coverage is required. It uses no filters. If one limits the exposure time to less than 2 minutes (which is a good compromise between limiting magnitude around 20.5 and sky coverage), then it is possible to take 30 frames per

hour. This would be done using the RA shift method, where the telescope is shifted one field to the east, while the CCDs are being readout in 10 seconds. This would allow to cover 75 square degrees per hour, or 600 square degrees per 8 hours night, corresponding to 18.1 gigabytes per night, or almost 32 gigabytes, or 6 Exabyte tapes in the best (or worse ?) case of 14 hours winter nights. This corresponds to the price of half a photographic plate.

Single triple CCD control module



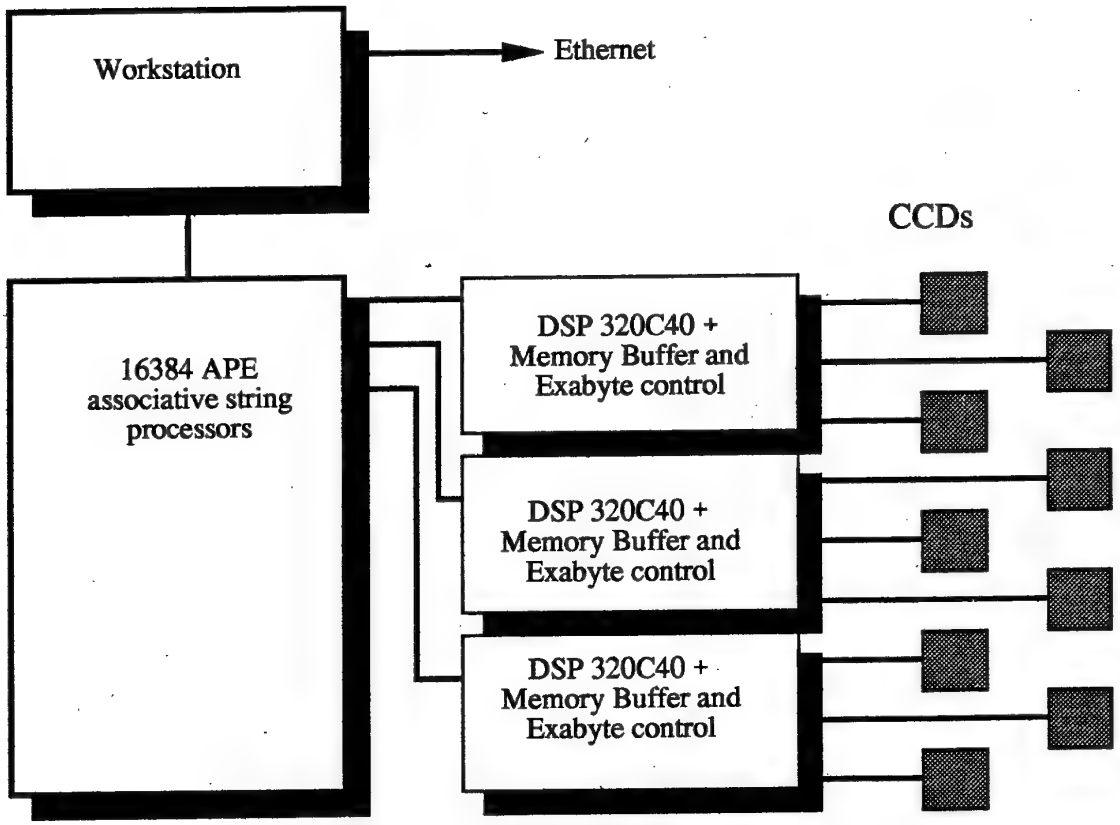
Pushing this system to its limit, it is possible to think to the detection of fast moving near Earth objects where a long exposure time is unnecessary (an object with a 5 degrees per day motion stays on the same pixel only 5 seconds). The main limitation in this system is the Exabyte trasnfert time, which ought to be around 50 seconds, and which we are aiming to reduce at only 25 seconds. Using the system at these high speed would result in the following values :

Exposure time hourly sky cov. 8 hours 14 hours

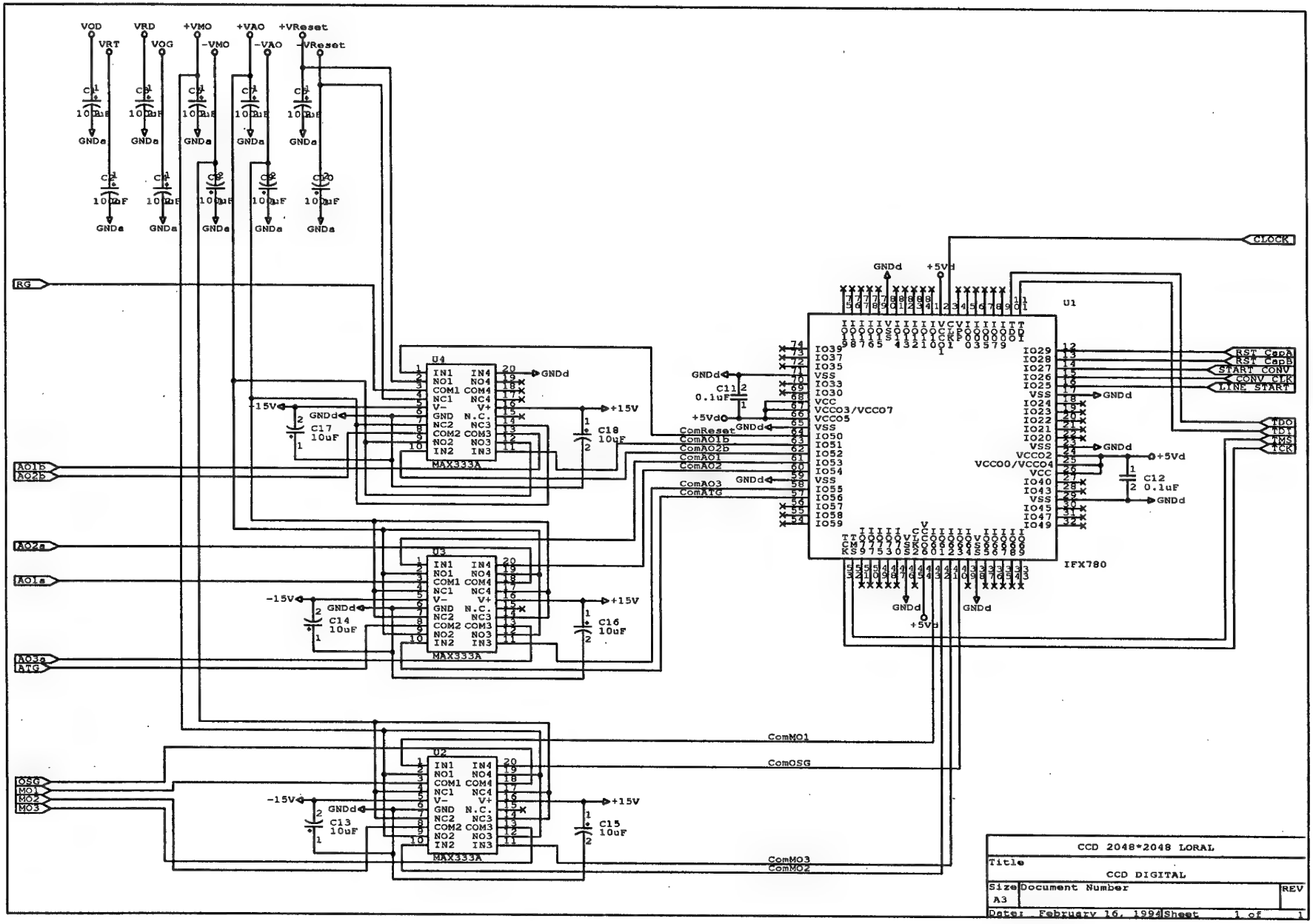
120	7.5	600	1050
60	150	1200	2100
35	257.5	2060	3605

It should be noted that the whole sky is around 41000 square degrees, so these high speed modes, provided a real time reduction engine was available could cover one twentieth to one tenth of the visible sky per night with a limiting magnitude around 20 or 19 respectively.
Such a system ought to be able to cover the whole sky visible from a given observatory in a matter of a dark run (or to generate this amount of data, even if it takes 2 years of calculation for a workstation to go through all the reduction...)

38 Megapixels camera with real time reduction



Appendix 1 : Electronic Schematics of the controller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+VAO
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ATG
OSG
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COM1 COM4
NC1 NC4
V- V+
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ComMO3
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U1
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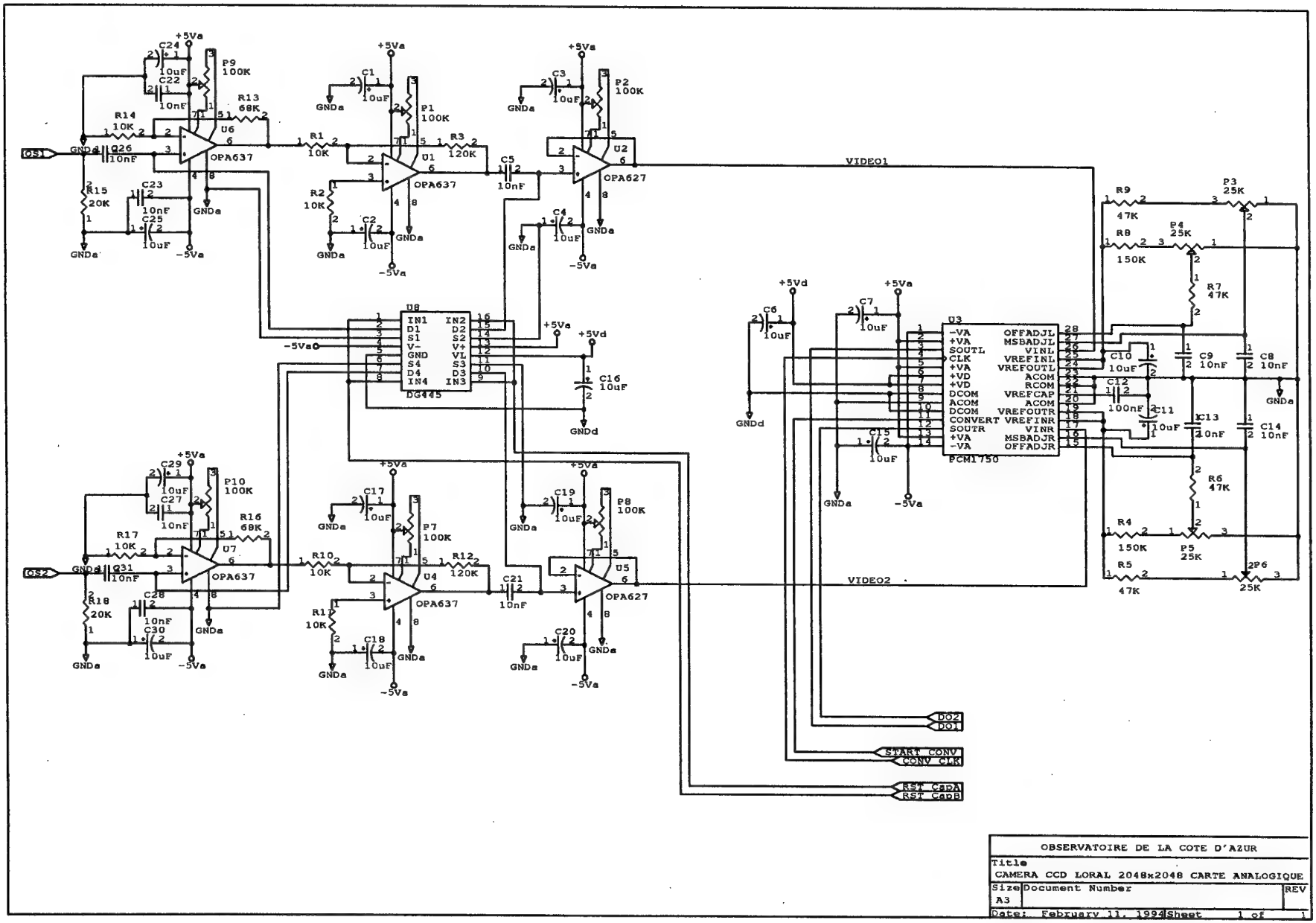
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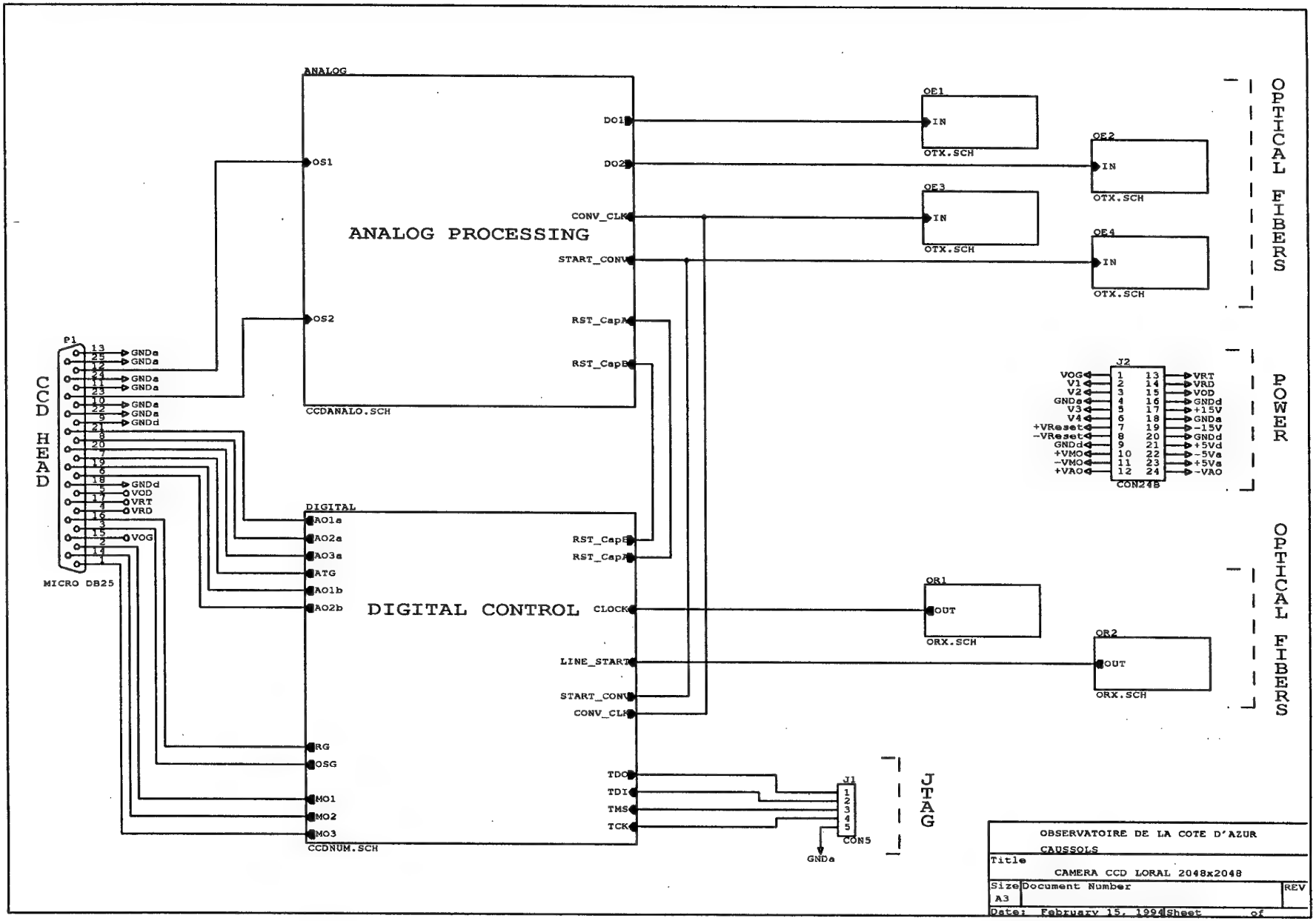
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DIGITAL CONTROL
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AO2a
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ATG
AO1b
AO2b
RG
OSG
MO1
MO2
MO3
CLOCK
LINE_START
OR1
OR2
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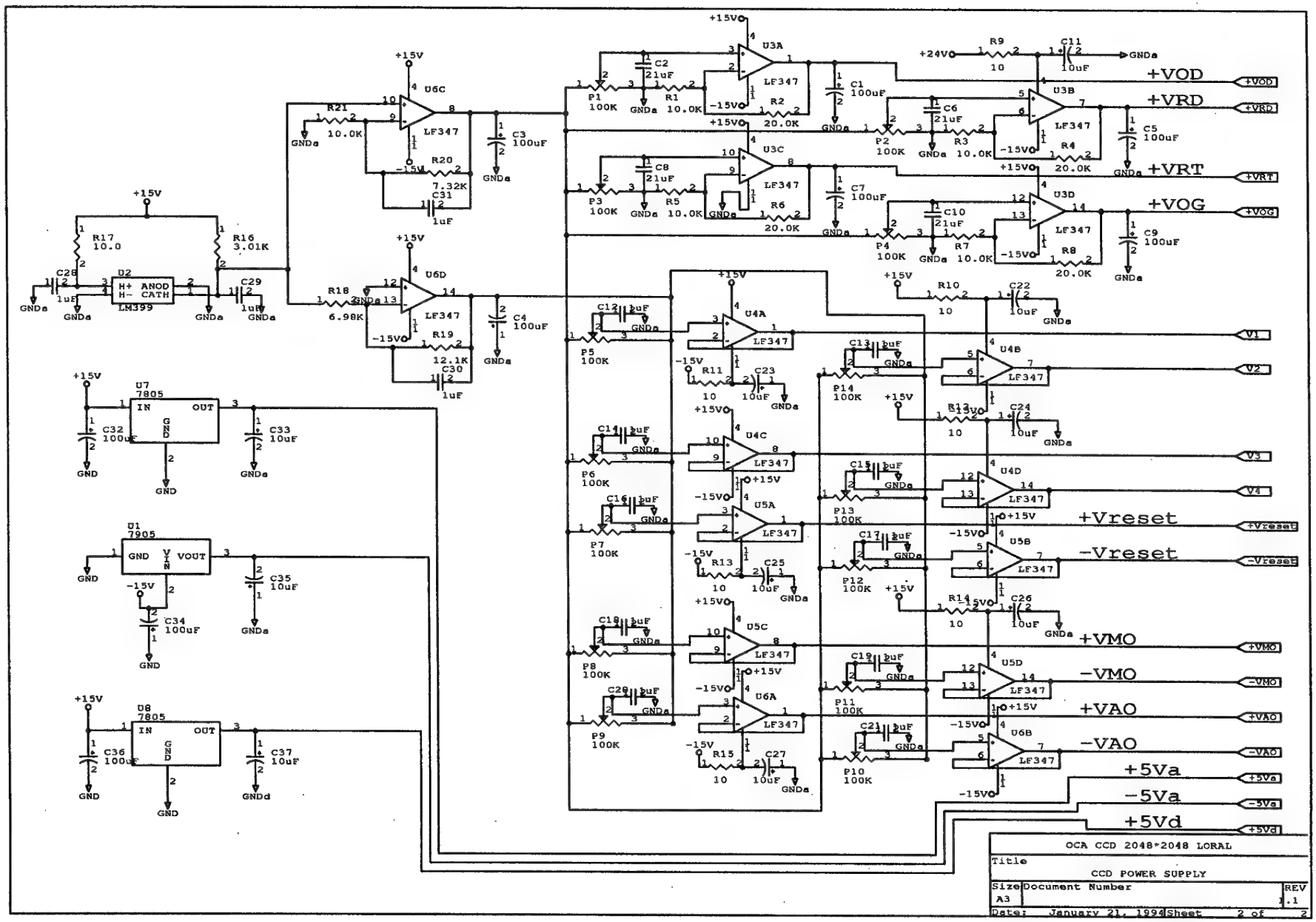
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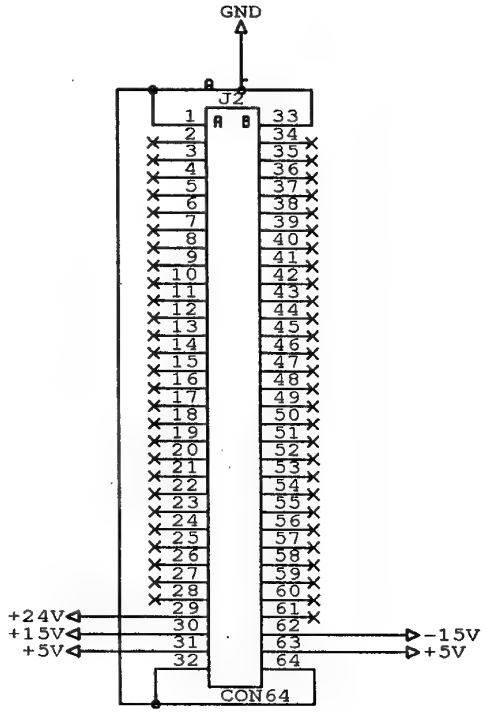
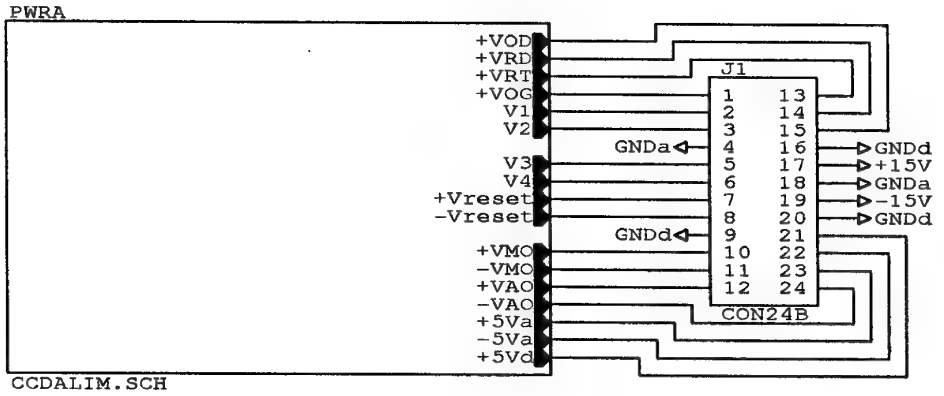
+VRD
+VRT
+VOG
V1
V2
V3
V4
+Vreset
-Vreset
+VMO
-VMO
+VAO
-VAO
+5Va
-5Va
+5Vd
OCA CCD 2048*2048 LORAL
CCD POWER SUPPLY
A3
REV 1.1
January 21, 1994
Sheet 2 of 2





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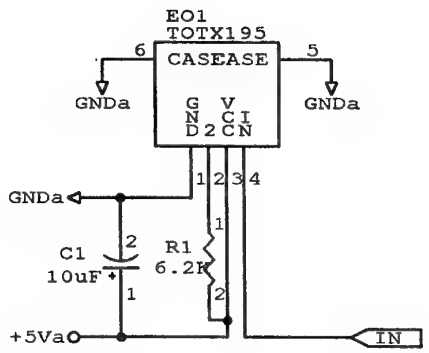

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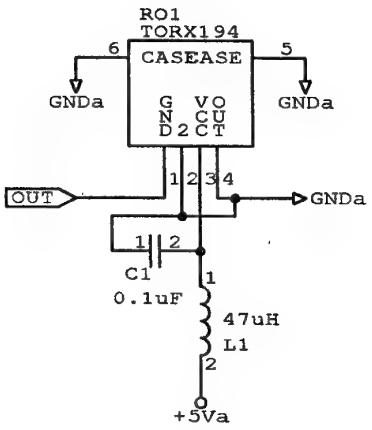
Size: A4	Document Number	REV
Date: February 7, 1994	Sheet of	



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Size A4	Document Number	REV
Date: February 9, 1994	Sheet of	

Appendix 2 : Data sheets of the main components of the controller

CCD442(FA2048) SPECIFICATIONS

ARRAY FORMAT	2048 X 2048
PIXEL SPACING	15 MICRONS HORIZONTAL AND VERTICAL
IMAGING AREA	30.7 MM X 30.7 MM
CCD TECHNOLOGY	THREE-PHASE BURIED CHANNEL NMOS
ARCHITECTURE	FULL FRAME
OUTPUT RATE	2.5 MHz MAXIMUM
NUMBER OF OUTPUTS	TWO
QUANTUM EFFICIENCY	SEE PLOT FOR FRONTSIDE ILLUMINATION
PIXEL UNIFORMITY	+/-5 PERCENT
RESPONSIVITY	1.0 V/MICROJOULE/CM**2
READOUT NOISE	<5e- RMS (4E-6SEC S/H TIME)
OUTPUT AMP SENSITIVITY	>0.6 E-6 VOLTS PER ELECTRON
EXTERNAL LOAD RESISTOR	3-20 K OHMS
POWER DISSIPATION	SEE GRAPH
D.C. OUTPUT LEVEL	14 VOLTS
PACKAGE	AUGAT ISOTRONICS PI-4950S-1
DEVICE MOUNTING	SILVER-FILLED EPOXY
DEVICE MATERIAL	FOUR-INCH 30-50 OHM-CM EPI SILICON
PROCESSING	2.5 MICRON MINIMUM GEOMETRIES TRIPLE-POLY SINGLE METAL

OPERATING MODES

	BURIED CHANNEL(MPP)	SURFACE CHANNEL
CHARGE CAPACITY	100,000e-	400,000e-
DARK CURRENT	<25pA/cm**2	<2nA/cm**2
OPERATING VOLTAGES	SEE TABLE	
OPERATING TEMPERATURE	25 C	
C.T.E.	>0.99999	SEE PLOT

The FA2048 is a 2048 x 2048 element solid state charge coupled device area image sensor which is intended for use in high resolution detector imaging systems and a variety of scientific and industrial optical instrumentation systems. The FA2048 is organized as a matrix array of 2048 horizontal lines by 2048 vertical columns of charge-coupled photoelements. The pixel spacing is 15 microns by 15 microns.

Excellent low noise performance is achieved by use of a buried channel CCD structure and a single stage low noise output amplifier. An additional implant under one array phase allows charge integration with all vertical array phases off which decreases dark current 100 fold.

Device processing is done using 2.5 micron design rules. The single-metal, triple-poly process allows three phase CCD layout with smaller pixel geometries and fewer array blemishes.

VERTICAL ARRAY CLOCKS A1,A2, and A3 are polysilicon gates used to transfer charge down the buried channel to the horizontal CCD

multiplexer. Vertical columns are separated by a channel stop region. Incident photons pass through the gate structure, are absorbed in the silicon crystal structure and create electron-hole pairs. The resulting photoelectrons are collected by the photosites during the integration time. An implant under one of the array phases creates a virtual well which collects the photoelectrons even with all the gates in the low(collapsed) state. This multi-pinned phase mode greatly decreases dark current generation in the integration mode. To increase charge capacity, the device may be operated by conventional methods by keeping one of the array phases on(high) during integration. The CCDs may be clocked at larger voltage levels, thus operating in surface channel mode, to increase charge handling capability.

The imaging array is divided into an upper and lower half. Each 1024 X 2048 half may be clocked independently or together. A serial CCD along the top and one along the bottom make it possible to clock each half out simultaneously or, if desired, the entire array out one side. The packaging pinouts are arranged so that the device may be rotated 180 degrees without changing timing by using the other serial mux. The Array Transfer Gate is the final array gate before charge is transferred to the serial multiplexer. For simplified timing, and fewer clocked lines the ATG may be tied to A2.

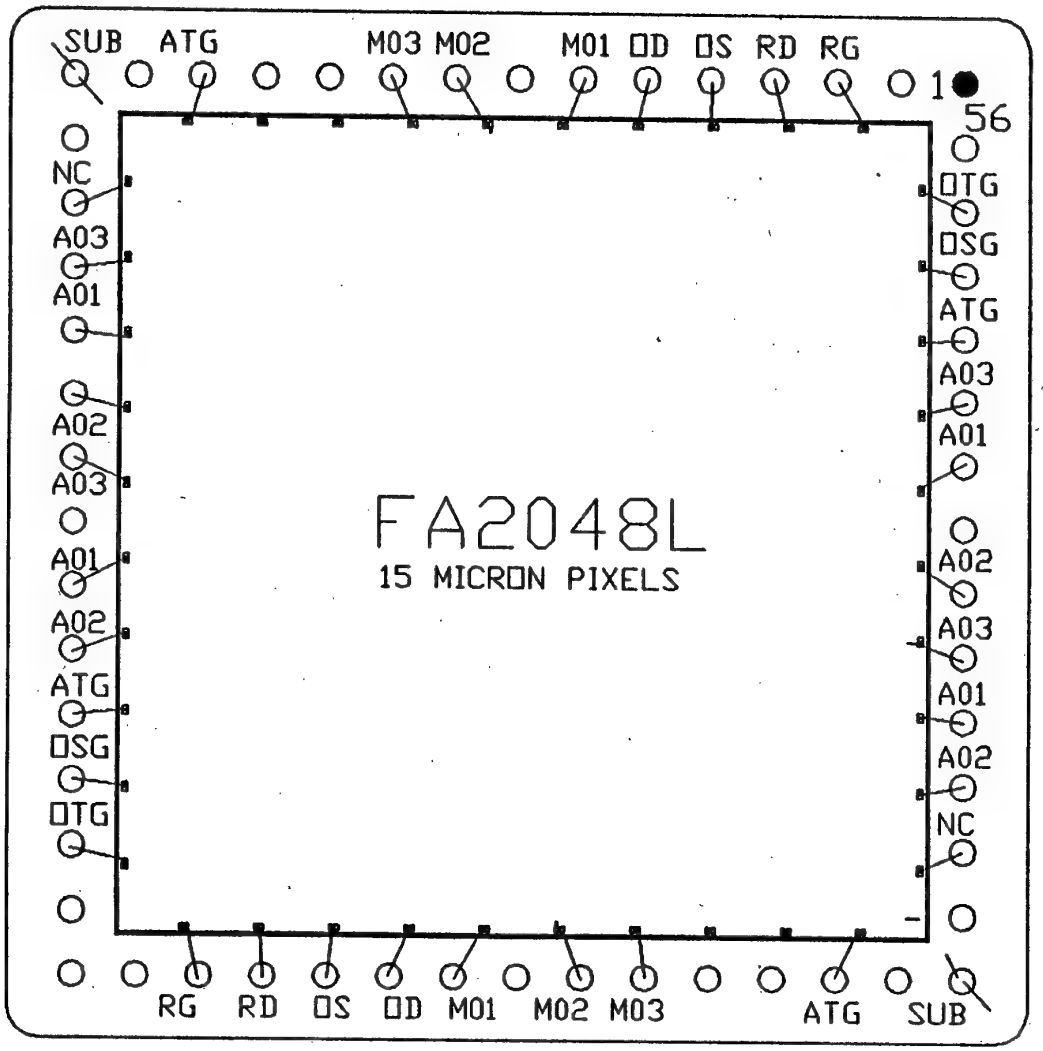
HORIZONTAL ARRAY CLOCKS M1,M2, and M3 are polysilicon gates used to transfer charge down either of the two horizontal buried channel CCDs to the output amplifier. The channels are twice the size of the vertical CCD channel to permit binning of charge. With binning, the array can be operated normally(2048 X 2048), as a 1024 X 2048 or binned as a 1024 X 1024 device. The transfer from the vertical array is into phases two and three of the horizontal CCD. The horizontal multiplexer has 16 additional "pixels" between the array and the output amplifier. The output from these transfers contain no signal and may be used as a dark level reference. The last gate in the horizontal multiplexer is sized twice as large as the other gates and can be used to bin charge from adjacent columns.

OUTPUT AMPLIFIER The FA2048 has two output amplifiers, one at the end of each serial multiplexer. Each is a single FET floating diffusion amplifier with a reset MOSFET tied to its input gate. Charge clocked from the serial multiplexer changes the voltage on the output amplifier gate. It is reset by use of the reset MOSFET. The Output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the output of the device.

DEVICE GRADING Device grading helps establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as row and column outages, hot pixels(excess response) and dark pixels(reduced response). A blemish is defined as a deviation outside the arrays' specification for photoresponse uniformity.

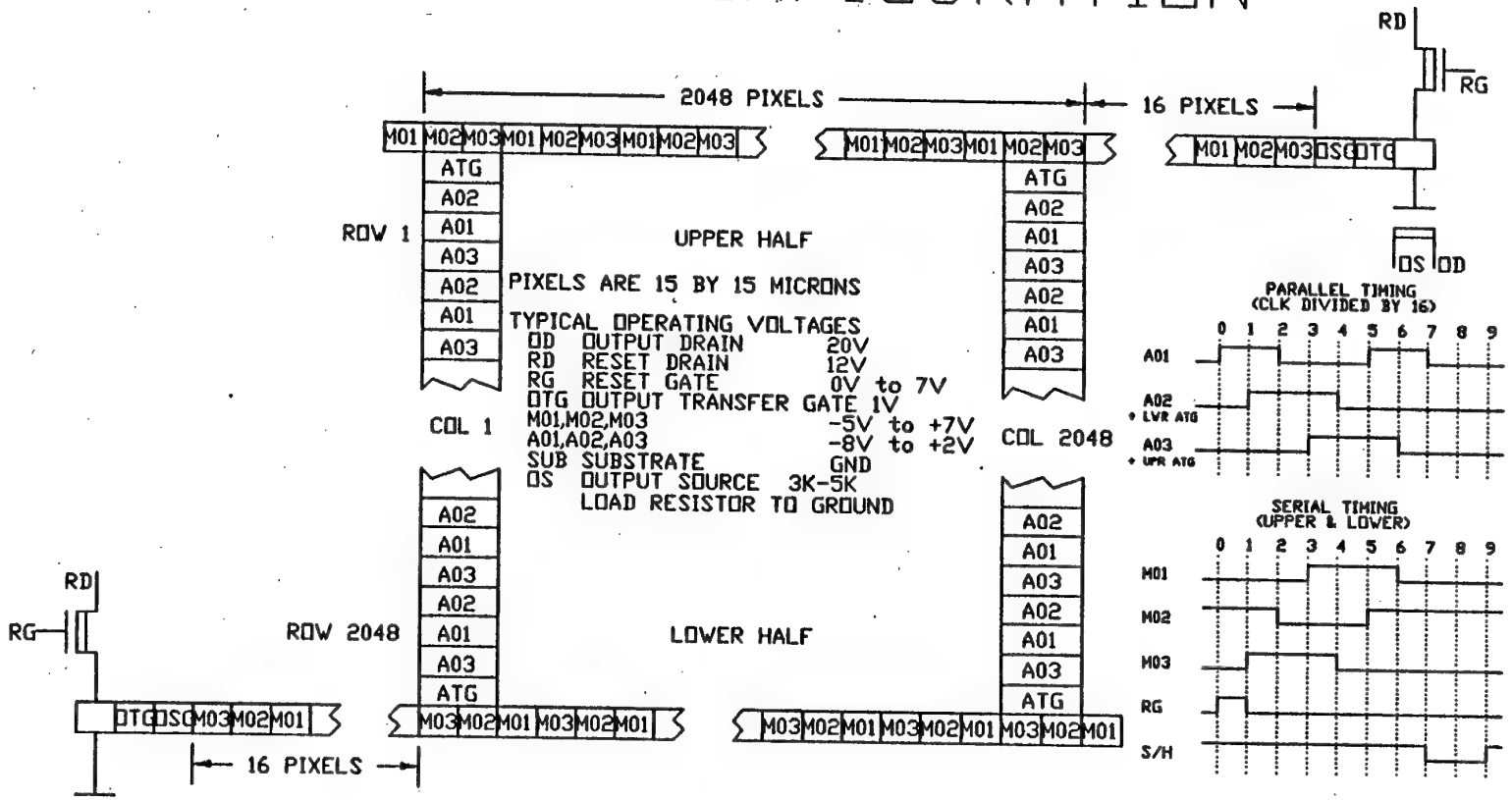
Blemishes are characterized in the central zone and for the total array. The central zone is defined as the middle 1024 X 1024 pixels. No row defects are permitted for any of our graded devices.

	CENTRAL ZONE		TOTAL ARRAY	
GRADE	PIXELS	COLUMNS	PIXELS	COLUMNS
0		DEFECT FREE		
1	40	2	100	5
2	100	8	300	30
3	300	15	500	60



3	RG	31	RG
4	RD	32	RD
5	ΦS	33	ΦS
6	ΦD	34	ΦD
7	M01	35	M01
9	M02	37	M02
10	M03	38	M03
13	ATG	41	ATG
15	SUB	15	SUB
17	NC	45	NC
18	A03	46	A02
19	A01	47	A01
20	A02	48	A03
21	A03	49	A02
23	A01	51	A01
24	A02	52	A03
25	ATG	53	ATG
26	ΦSG	54	ΦSG
27	ΦTG	55	ΦTG

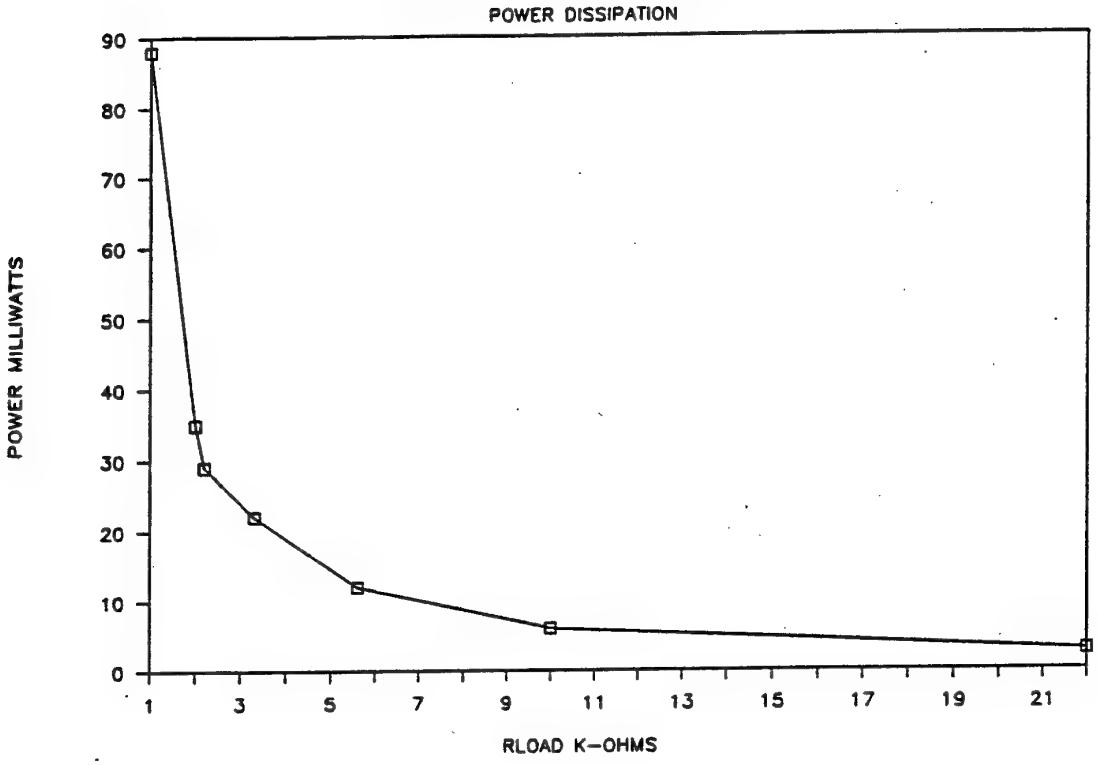
FA2048L CONFIGURATION

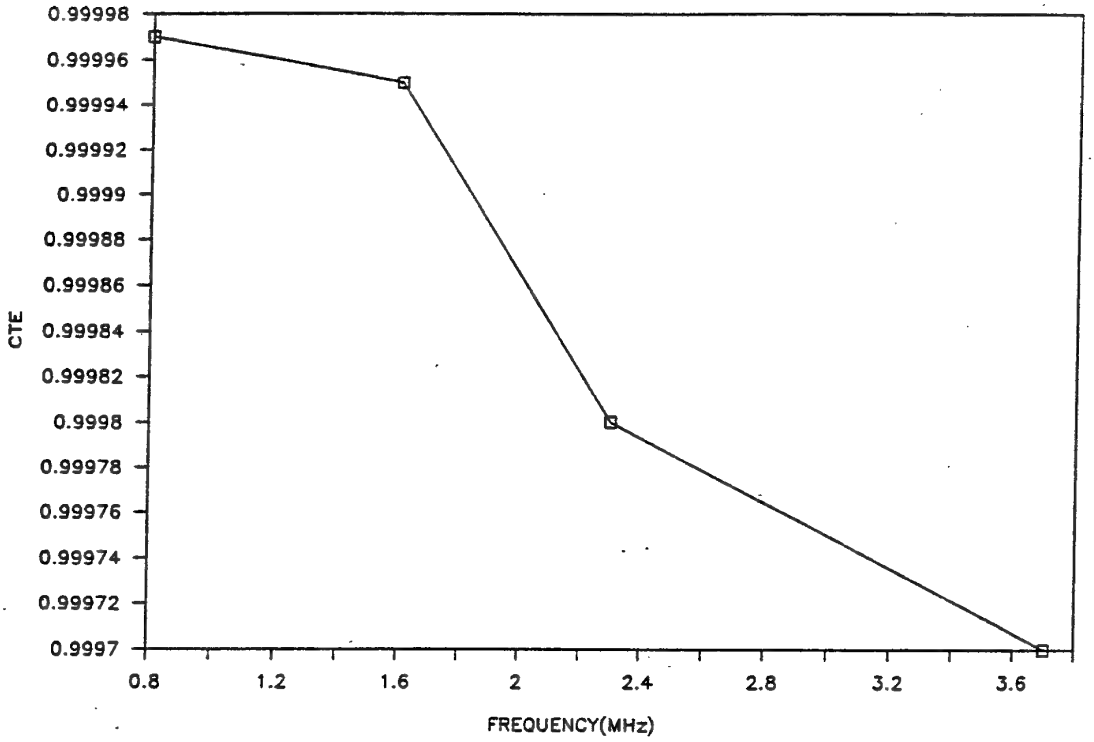


* NOTE: OSG should be tied to M01 of both serial registers if the pixels are not summed.

* NOTE: To avoid separate clocking the upper ATG can be tied to A03 and the lower ATG tied to A02.

OUTPUT AMPLIFIER

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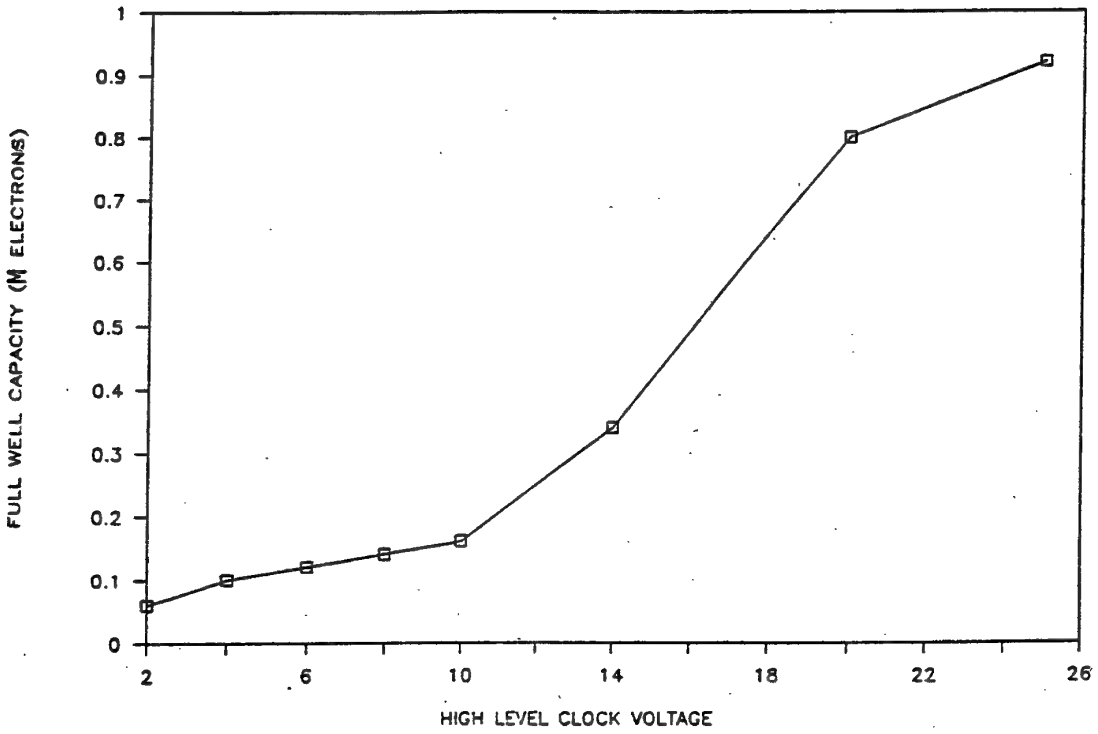
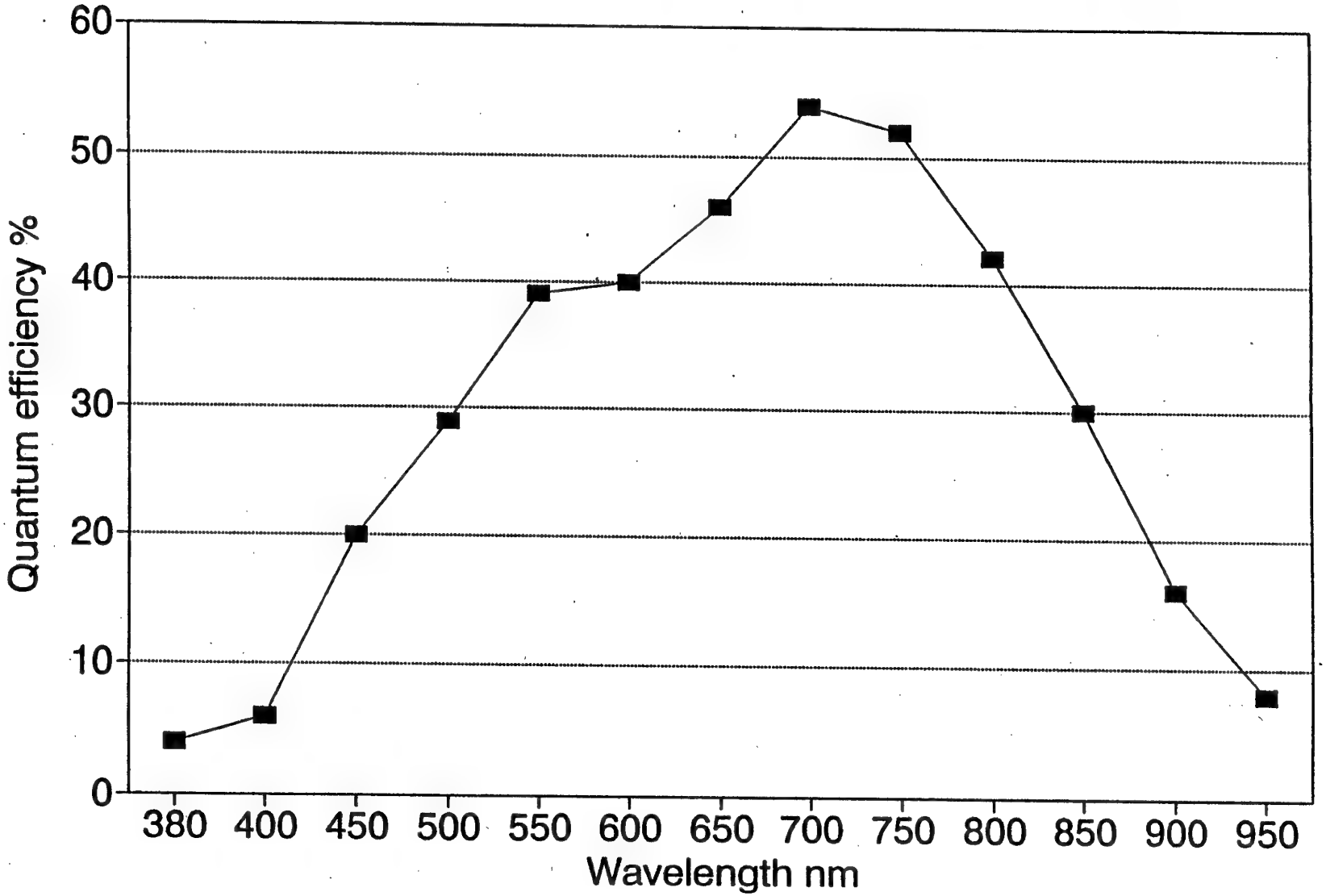
0.99996
0.99994
0.99992
0.9999
0.99988
0.99986
0.99984
0.99982
0.9998
0.99978
0.99976
0.99974
0.99972
0.9997
CTE
0.8
1.2
1.6
2
2.4
2.8
3.2
3.6
FREQUENCY(MHz)


1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
FULL WELL CAPACITY (M ELECTRONS)
2
6
10
14
18
22
26
HIGH LEVEL CLOCK VOLTAGE

TYPICAL LORAL LARGE AREA
IMAGER QUANTUM EFFICIENCY



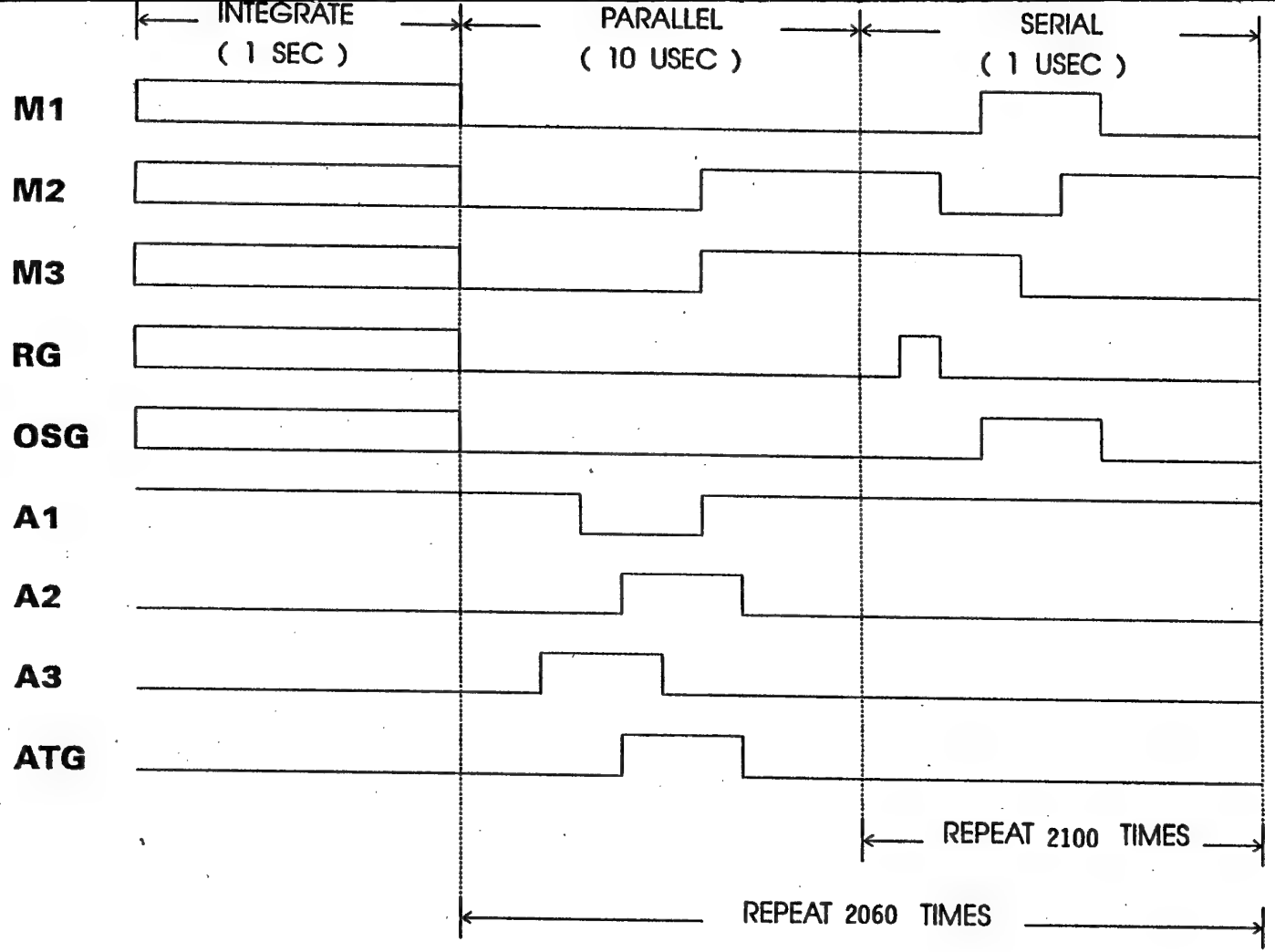
TYPICAL OPERATING VOLTAGES

	Burried Channel (MPP)		Surface Channel	
	HIGH	LOW	HIGH	LOW
M1	+7	-4	+16	0
M2	+7	-4	+16	0
M3	+7	-4	+16	0
RG	+8	0	+12	0
OSG	+7	-4	+16	0
A1	+2	-8	+14	0
A2	+2	-8	+14	0
A3	+2	-8	+14	0
ATG	+2	-8	+14	0

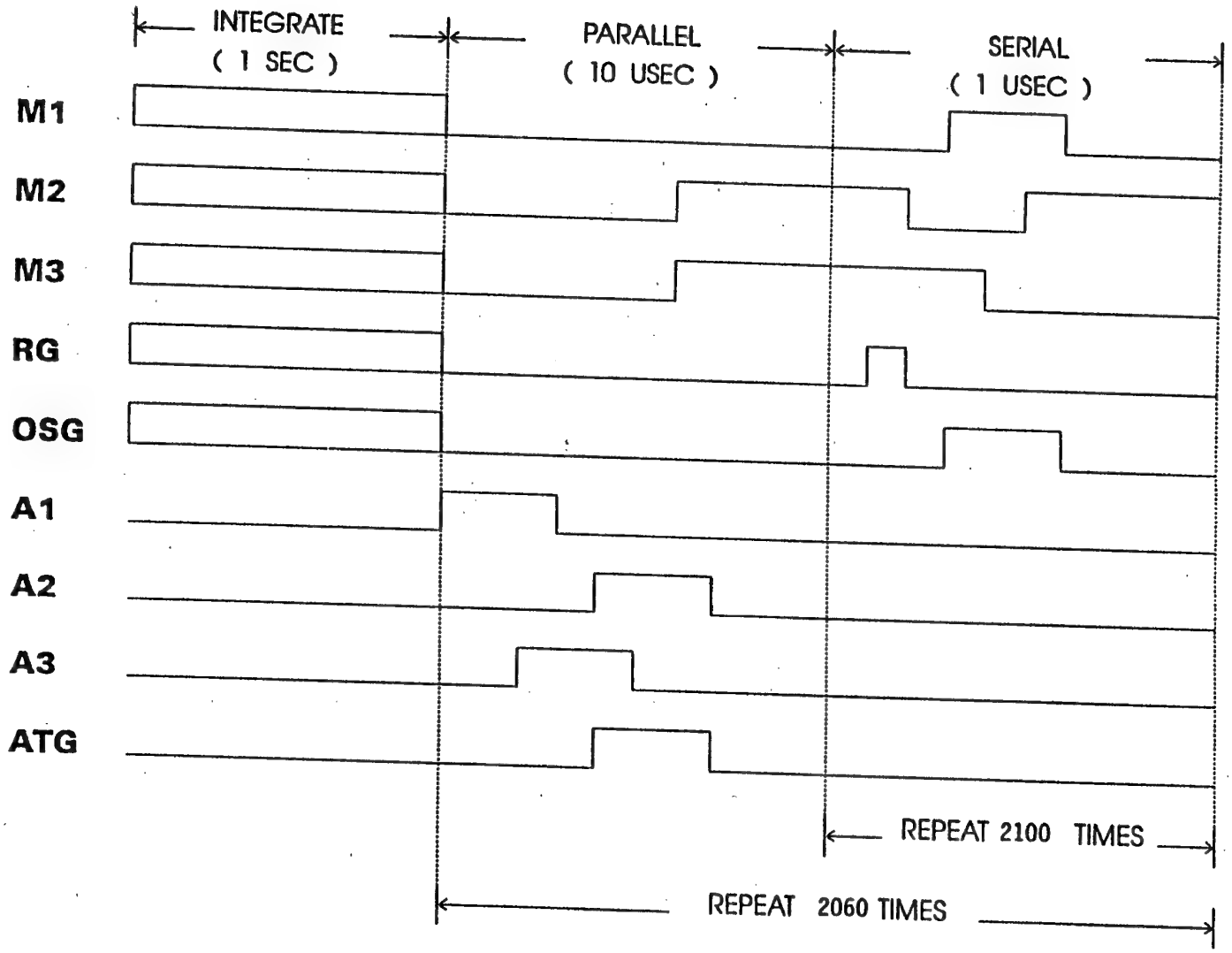
D.C. VOLTAGE LEVELS

OD	20
ORD	13
OTG	1.0

Substrate is Grounded



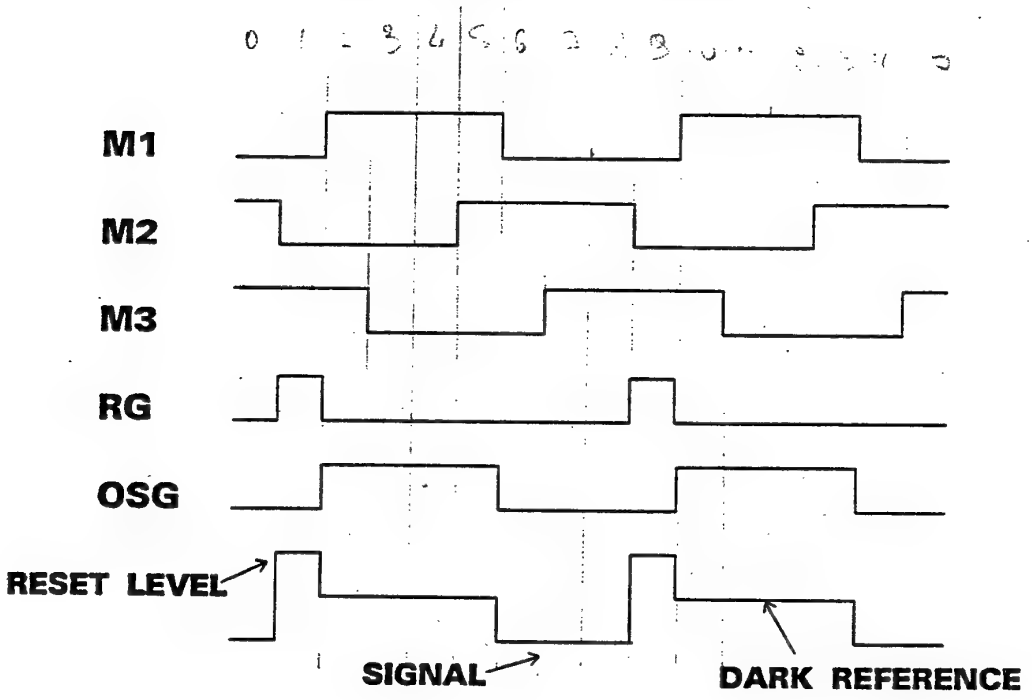
NON-MPP MODE OF OPERATION



MPP MODE OF OPERATION

OUTPUT (SERIAL) MUX OPERATION WITH TYPICAL OUTPUT

— 16 périodes



iFX780
10 ns FLEXlogic FPGA FAMILY WITH SRAM OPTION

- **High Performance FPGA (Field Programmable Gate Array)**
  - **— Deterministic 10 ns Pin-to-Pin Propagation Delays**
  - **— 80 MHz System Clock Frequency**
- **5,000 Equivalent Logic Gates or up to 10,240 Bits of SRAM**
- **0.8μ CHMOS* Technology**
  - **— Power Management Options Minimize Active Power Consumption (1.5 mA/MHz)**
  - **— Zero Power Standby**
- **JTAG 1149.1 Compatible Test Port**
  - **— Supports Boundary Scan and In-circuit Reconfiguration/Programming**
- **Eight Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix**
  - **— Improves Fitting of Complex Designs**
- **Any CFB can be either 24V10 Logic or SRAM Block**
  - **— Up to 80 Complex Macrocells**
  - **— 128 x 10 SRAM Configuration**
  - **— CFB Selectable 3.3V or 5V Outputs**
  - **— Open-Drain Output Option**
- **24V10 Macrocell Features**
  - **— Dual Feedback on All I/O Pins**
  - **— Allocation Supports up to 16 Product Terms Per Macrocell with No Performance Penalty**
  - **— 12 Clocking Options**
  - **— Flexible Preset/Clear Options**
  - **— Selectable D/T/JK/SR Flip-Flops**
  - **— Fast 12-Bit Identity Compare Option**
- **Supported by Industry Standard Design and Programming Tools**

2

290459-1

290459-2

Package Options

Pins	Package	Macrocells	I/O	Inputs	Clock	JTAG/V_{PP}	V_{CC}	GND
84	PLCC	80	60	0	2	5	8	9
132	PQFP	80	80	22	2	5	10	13

*CHMOS is a patented process of Intel Corporation.

October 1992
Order Number: 290459-002

INTRODUCTION

The iXF780 is the first member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The iFX780 consists of eight configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128 x 10 SRAM. This combination will provide approximately 5,000 gates of logic in either PLCC or PQFP packages.

Flexible Performance

The iFX780 uses Intel's 0.8μ CHMOS EPROM technology to provide an 80 MHz external clock frequency with predictable 10 ns pin-to-pin delays. This advanced process technology combined with power management options enables very low active and standby power consumption.

Flexible Features

The unique combination of features available in the iFX780 make it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache control, and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the iFX780 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication controllers or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design itself.

Flexible Testing and Programming

The iFX780 also provides dedicated JTAG 1149.1 compatible pins to support boundary scan, in-circuit reconfiguration, and programming modes. In-circuit reconfiguration not only allows the designer ultimate flexibility in prototyping new designs, but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the iFX780 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time.

Flexible Tools Support

The FLEXLogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus™ software. This software runs on I386TM or higher PC-compatible platforms.

INTERCONNECT

The Global Interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

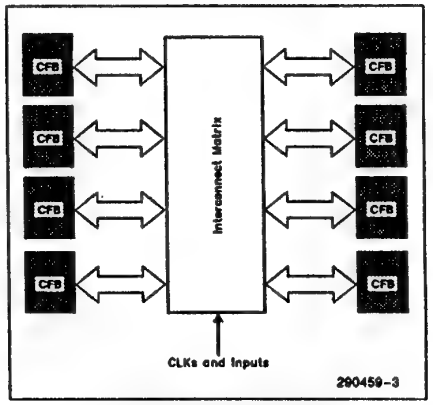


Figure 1. Interconnect Matrix

CONFIGURABLE FUNCTION BLOCKS

24V10 Mode

Each 24V10 block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a superior fan-in to macrocell ratio (2.4:1). This improves the fitting capacity of the iFX780 architecture by providing more available interconnect lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

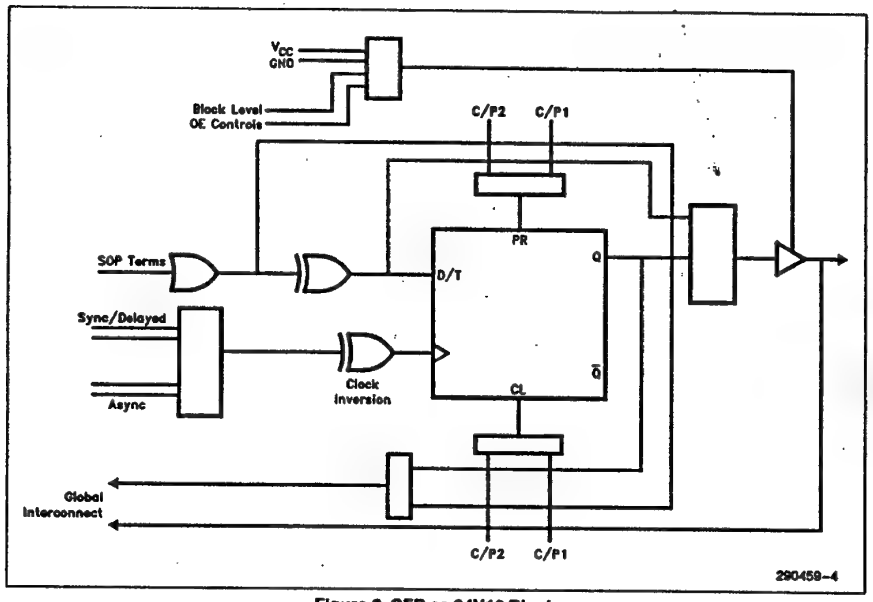


Figure 2. CFB as 24V10 Block

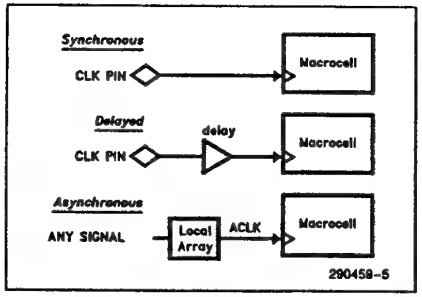


Figure 3. Clocking Modes

Macrocell Configurations

Each I/O of the device has dual (internal and pin) feedback paths shown in Figure 2. This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Depending on the package used, some macrocell outputs may not be brought outside the package. These I/Os may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available as software emulations.

Clocking Modes

There are three clocking modes available for every macrocell (see Figure 3): *synchronous, delayed, and asynchronous*. Table 1 shows the different timing options each clock mode offers.

Synchronous is the standard clock mode where the register clock is driven directly from one of the two global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Table 1. Clock Mode Timings

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	6.5	0	6
Delayed	5	2	8
Asynchronous	2	5	12

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

Control Signals

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

Comparator Logic

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals, within the T_{PD} of the device.

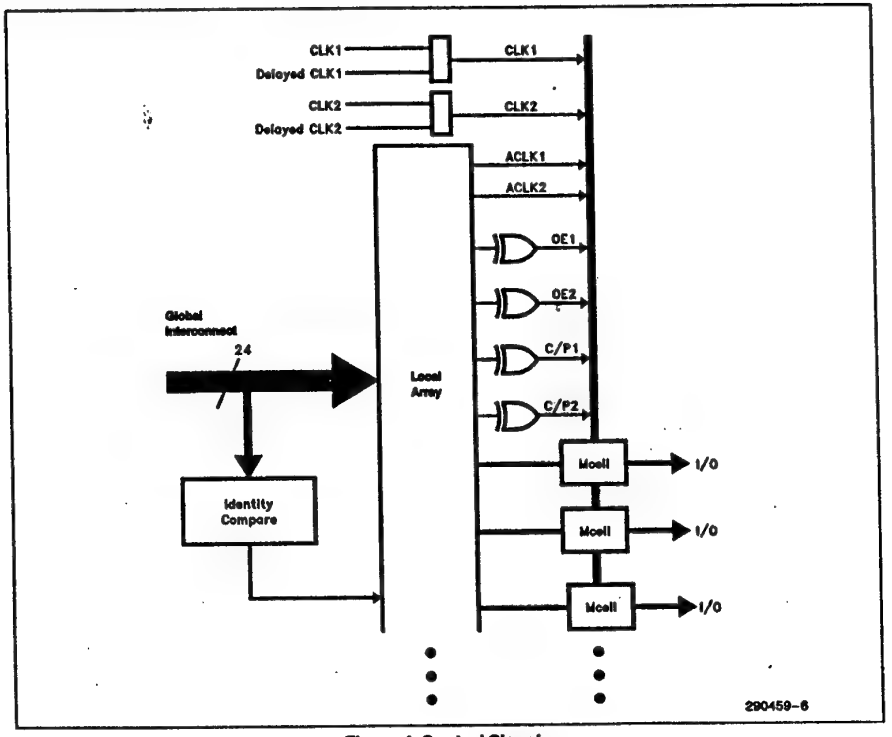


Figure 4. Control Signals

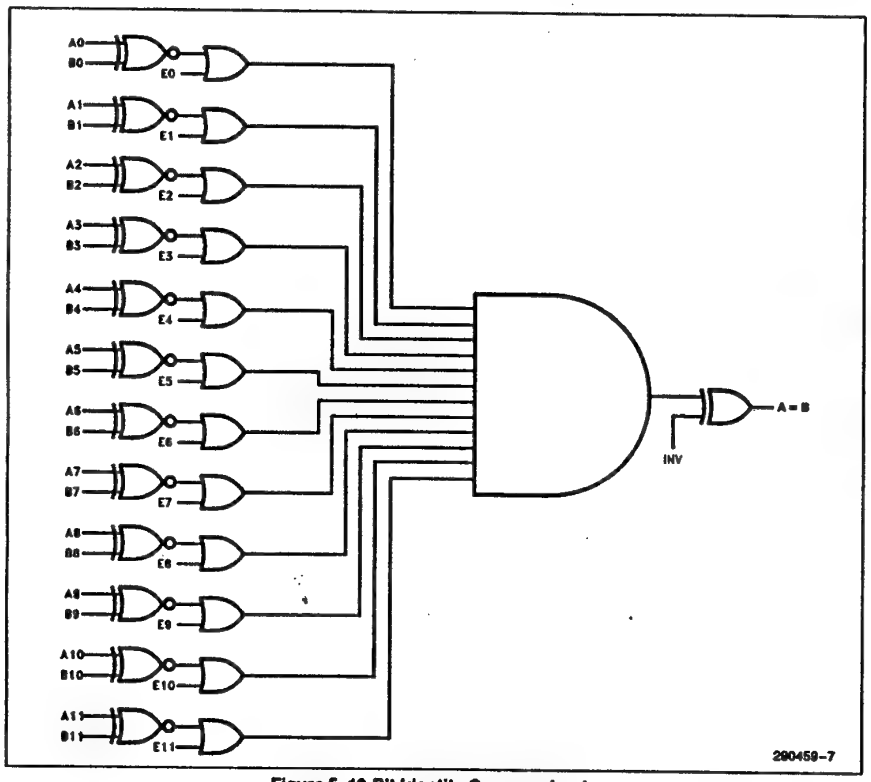


Figure 5. 12-Bit Identity Compare Logic

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24–16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

Product Term Allocation

The iFX780 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 or 16 P-terms are being used.

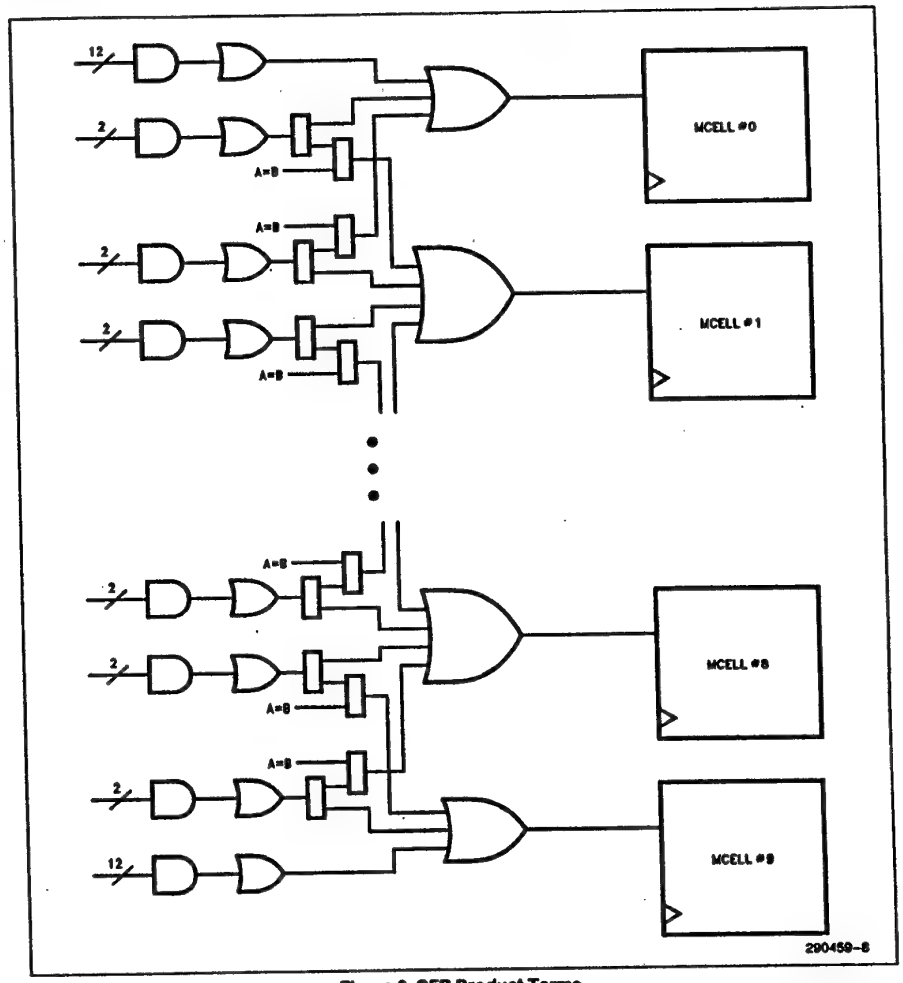


Figure 6. CFB Product Terms

SRAM Configuration

Each iFX780 CFB block can be configured as a 128x10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for $\overline{BE}$, $\overline{WE}$, and $\overline{OE}$ controls (see Table 2).

Table 2. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$	$\overline{WE}$	$\overline{OE}$		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip non-volatile configuration cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the macrocells and P-terms have been converted to SRAM use.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

Input Configuration

The iFX780 can be configured to enable a weak feedback pullup option on any CFB input. This option can be used to reduce power consumption for 5V inputs but may increase leakage currents during input transitions.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the iFX780 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block. This allows the iFX780 to be used in mixed voltage systems. For example, the iFX780 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

Power sequencing *is* required when any or all CFBs operate at 3.3V levels. In this case, the 5V source must be equal to or greater than the 3.3V source during power-up. During power-down, the 3.3V source must be less than or equal to the 5V source.

Open Drain Output Option

The device can also be configured to enable an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL versus CMOS Outputs

There is a weak pullup provided for CMOS compatible outputs. This pullup is always active in both 3.3V and 5V modes.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the iFX780. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The iFX780 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The boundary scan cells of the iFX780 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the iFX780 for prototyping new system designs.

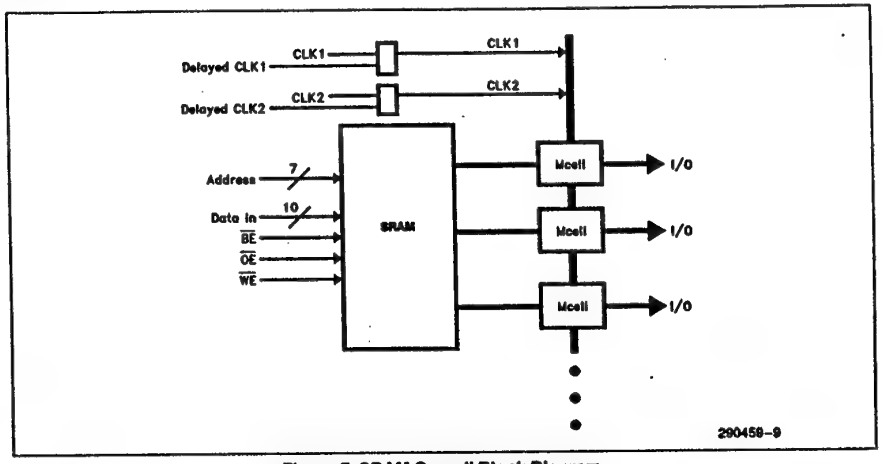


Figure 7. SRAM Overall Block Diagram

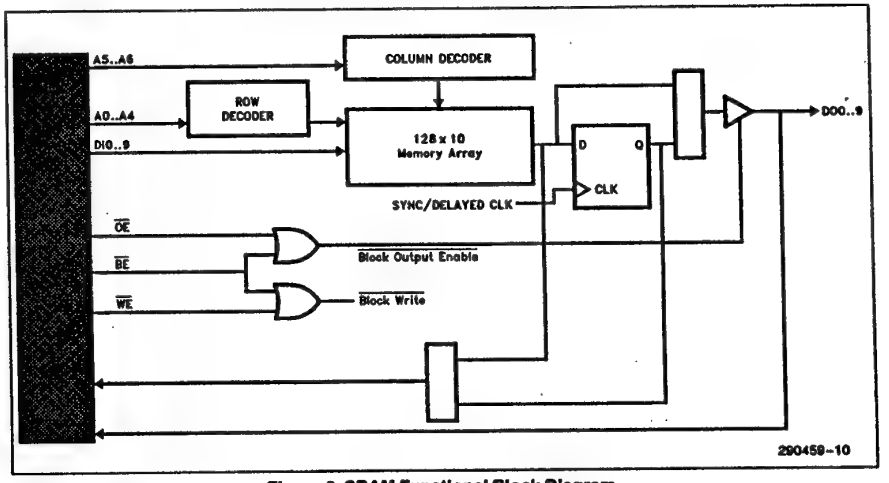


Figure 8. SRAM Functional Block Diagram

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit programming.

Boundary Scan Instructions

The iFX780 boundary scan Instruction Register (IR) supports public instruction opcodes, "semi-public" instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR Opcode 00000 Binary)

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the iFX780 package, typically for printed circuit board interconnects.

BYPASS (IR Opcode 11111 Binary)

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR Opcode 00001 Binary)

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a "snap-shot" of the values of the pins of the iFX780 in an unobtrusive manner and 2) preloads data to the iFX780 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR Opcode 00010 Binary)

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the IDcode to be serially shifted out of TDO.

UESCODE (IR Opcode 10110 Binary)

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR Opcode 01000 Binary)

The HIZ instruction sets all I/Os to a high impedance state.

IN-CIRCUIT RECONFIGURATION

The iFX780 supports in-circuit reconfiguration and in-circuit programming through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device.

This may be done as many times as desired in a prototyping scenario. Once the final version of the design is confirmed it may be programmed into the non-volatile cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pin (V_{pp}).

For more details on in-circuit reconfiguration and programming please refer to the iFX780 Device Programming and In-Circuit Reconfiguration Specification and supporting application notes.

2

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the non-volatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus includes several enhancements over earlier versions:

— Design Merge
— SRAM Configuration Support
— Compare Operation Support
— Simulation Support for Intel FPGA
— Vector Notation
— Full Mouse Support
— Device Selector

Design Merge

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel iFX780. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA Architectural Feature Support

PLDshell Plus supports all of the innovative architectural features of the iFX780 through the implementation of new language syntax such as:

— SRAM configuration
— Compare operation
— Buried macrocells
— Clocking options
— 3.3V and 5V options

Functional Simulation

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

— Event-driven simulation of combinatorial, registered, and state machine designs
— Ability to set any input, preload any register, and compare any output against an expected value
— Ability to group signals together (form a vector) to simulate a bus
— Generation of test vectors from simulation results for inclusion in the JEDEC file
— Simulation history file with ability to output a subset of signals to a secondary trace file

Device Selector

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

System Requirements

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

— Intel 386 based PC compatible
— 2MB RAM (minimum)
— VGA monitor/adaptor
— DOS 3.1 (or later)

THIRD-PARTY SUPPORT DESIGN SOFTWARE

Third party tools support will be provided by the following vendors:

- Acugen
  - — ATGEN™ Test Generation: Automatically generates high coverage functional test vectors for programmable logic devices.
- Cadence
  - — Composer™: Comprehensive suite of design entry, debug and documentation capabilities.
  - — Verilog-XL™ and VHDL-XL™: Digital logic simulators and interactive debug environment.
- Data I/O
  - — ABEL™: Design software allowing you to describe and implement logic designs.
  - — PLDtest™ Plus: Integrated software package that combines a testability analysis of the device under design or test with fault grading and automatic test vector generation.
- Logical Devices
  - — CUPL™: High level, universal design software package.
- Mentor Graphics
  - — Design Architect™: Integrated system of schematic, symbol, and text editors for capturing designs.
  - — QuickSim™: High performance logic simulator for function and performance verification.
- Minc
  - — PLDesigner-XL(R): Powerful design tool that can be used for all types of programmable logic with automatic device selection, automatic partitioning and functional simulation.
- OrCAD
  - — PLD Tools & Schematic Design Tool™: Software tool environment including schematic entry, test vector generation and multiple forms of input.
  - — Verification/Simulation Tool™: Series of software tools for performing timing-based simulation of designs.

- Quad Design
  - — MOTIVE™: Advanced timing verifier for identifying setup and hold violations in a design.
- Viewlogic
  - — ViewPLD & Powerview™: Integrated schematic capture and simulation environment.

PROGRAMMING SUPPORT

Programming Support will be provided following vendors:

- BP Microsystems
  - — PLD 1100
- Data I/O
  - — Unisite 2900/3900
- Elan
  - — Model 6000
- Logical Devices
  - — ALLPRO
- SMS
  - — Sprint Plus

DEVICE MODELS

Simulation models will be provided by the following vendors:

- Logic Modeling Corporation
  - — Smart Model: Device model support for behavioral simulation through a variety of simulators.
- Viewlogic

2

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	+7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	+13.5	V
V_I	DC Input Voltage(1, 2)	−0.5	V_{CC}+0.5	V
t_{STG}	Storage Temperature	−65	+150	°C
t_{AMB}	Ambient Temperature(3)	−10	+85	°C

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage - 5V	4.75	5.25	V
V_{CCO}	Output Supply Voltage - 3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_A	Operating Temperature	0	+70	°C
t_r	Input Rise Time		500	ns
t_f	Input Fall Time		500	ns

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)(4)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(5)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	5V TTL High Level Output	2.4			V	I/O = −4.0 mA D.C., V_{CC} = Min
	5V CMOS High Level Output	V_{CCO} −0.2			V	I/O = −20 µA D.C., V_{CC} = Min
	3V High Level Output Voltage	V_{CCO} −0.2			V	I/O = −20 µA D.C., V_{CC} = Min
V_{OL}	5V Low Level Output Voltage			0.45	V	I/O = 12.0 mA D.C., V_{CC} = Min
	3V Low Level Output Voltage			0.2	V	I/O = 20 µA D.C., V_{CC} = Min
I_I	Input Leakage Current			±10	µA	V_{CC} = Max, V_{IN} = GND or V_{CC}

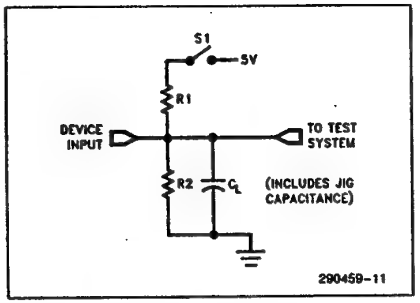
NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)[4] (Continued)

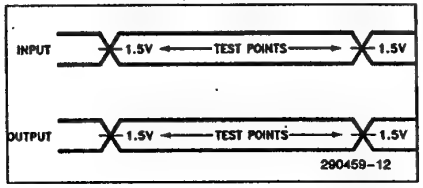
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = Max, V_{OUT} = GND or V_{CC}
I_{SC}[6]	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max, V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current		1		mA	V_{IN} = V_{CC} or GND, Outputs Open
I_{CC} Active	Power Supply Current		1.5		mA per MHz	V_{IN} = V_{CC} or GND, Outputs Open, Device Programmed as Four 20-Bit Counters

NOTE:
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



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SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial		Measured Output Value
			R1	R2	
t_{PD}	Closed	35 pF	330Ω	200Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

PIN CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)[7]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz		10	12	pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz		12	15	pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz		15	18	pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz		12	15	pF

NOTE:
7. These values are evaluated at initial characterization and whenever design modifications occur that may affect capaci-

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	IFX780-10			IFX780-15			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}[8]	Input or I/O to Output Valid			10			15	ns
t_{PZX}[9]	Input or I/O to Output Enable			12			18	ns
t_{PXZ}[9]	Input or I/O to Output Disable			12			18	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			15			20	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			10			15	ns

REGISTER MODE—IFX780-10 CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}[8]	Max Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	80		76.9		71.4		MHz
f_{CNT2}[8]	Max Counter Frequency $1/(t_{CNT})$—Internal Feedback	80		76.9		71.4		MHz
f_{MAX}[8]	Max Frequency (Pipelined) $1/(t_{CP})$—No Feedback	100		92.9		80		MHz
t_{SU}	Input or I/O Setup Time to CLK	6.5		5		2		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		6		8		12	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		16		18		22	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		12.5		13		14	ns
t_{CL}	CLK Low Time	4		4		5		ns
t_{CH}	CLK High Time	4		4		5		ns
t_{CP}	CLK Period	10		10.5		12.5		ns

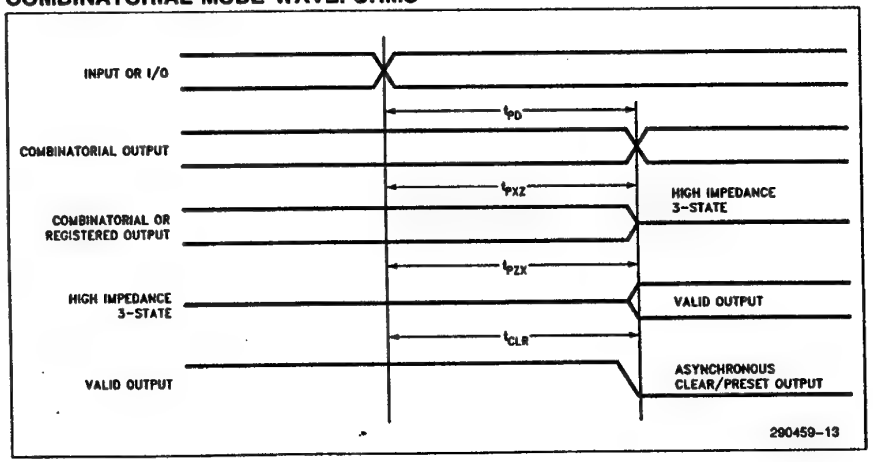
NOTES:
8. Half outputs switching per block.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measured with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

REGISTER MODE—IFX780-15 CLOCK A.C. CHARACTERISTICS

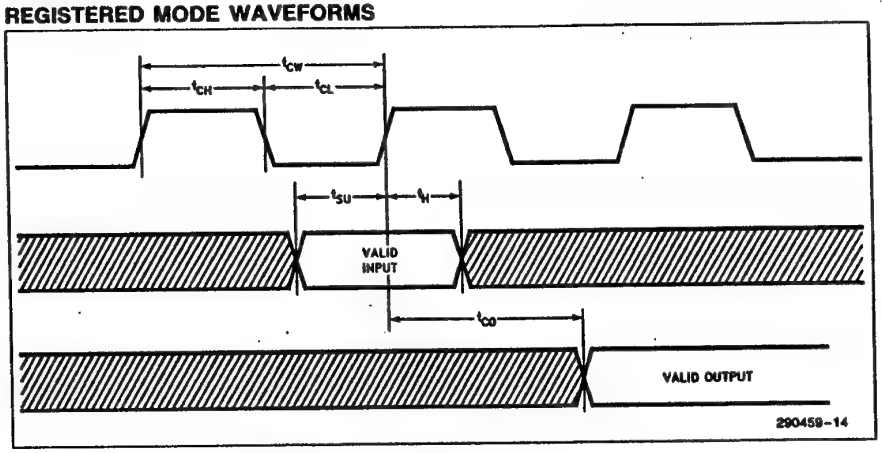
(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Synchronous		Delayed Sync		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	50		50		50		MHz
f_{CNT2}	Max Counter Frequency $1/(t_{CNT})$—Internal Feedback	50		50		50		MHz
f_{MAX}	Max Frequency (Pipelined) $1/(t_{CP})$—No Feedback	66.7		62.5		62.5		MHz
t_{SU}	Input or I/O Setup Time to CLK	11		8		3		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		9		12		17	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell		19		22		27	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		20		20		20	ns
t_{CL}	CLK Low Time	7		7		7		ns
t_{CH}	CLK High Time	7		7		7		ns
t_{CP}	CLK Period	15		15		15		ns

COMBINATORIAL MODE WAVEFORMS



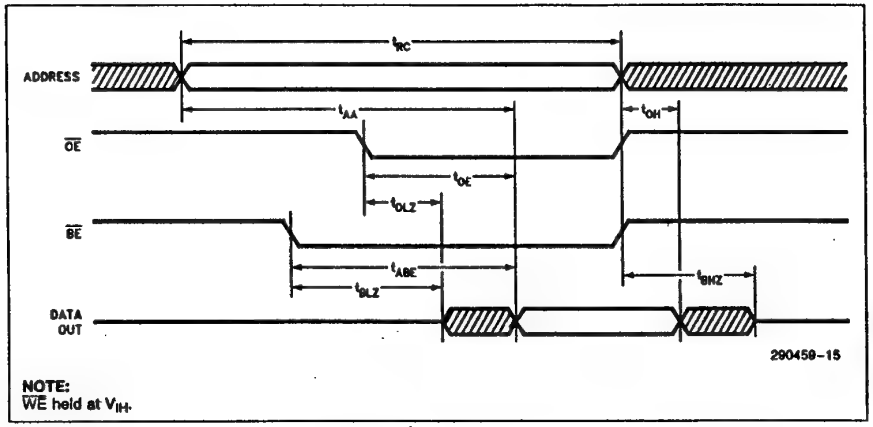
REGISTERED MODE WAVEFORMS



SRAM READ—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	IFX780-10		IFX780-15		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address Access Time		15		20	ns
t_{ABE}	Block Enable Access Time		15		20	ns
t_{OE}(1)	Output Enable to Output Valid		10		15	ns
t_{OH}	Output Hold from Address Change	2		3		ns
t_{BLZ}(1)	Block Enable to Output in Low Z	3		5		ns
t_{BHZ}(1, 2)	Block Disable to Output in High Z		10		15	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	3		5		ns

TIMING WAVEFORM OF READ CYCLE



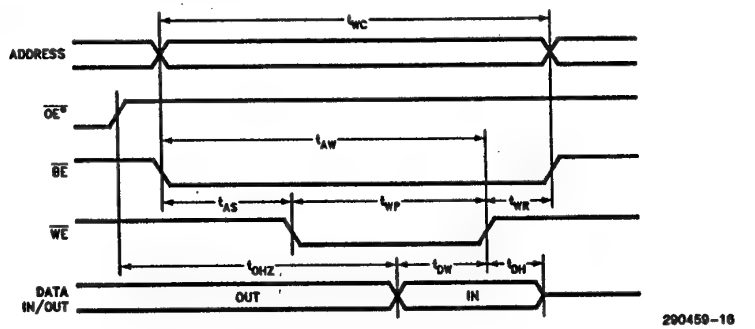
NOTE:
$\overline{WE}$ held at V_{IH}.

SRAM WRITE—A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	IFX780-10		IFX780-15		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		ns
t_{BW}	Block Enable to End of Write	12		16		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Set-up Time	3		4		ns
t_{WP}	Write Pulse Width	12		16		ns
t_{WR}	Write Recovery Time	0		0		ns
t_{DW}	Data Valid to End of Write	12		16		ns
t_{DH}	Data Hold Time	0		0		ns
t_{OHZ}(1, 2, 3)	Output Disable to Valid Data In	10		13		ns

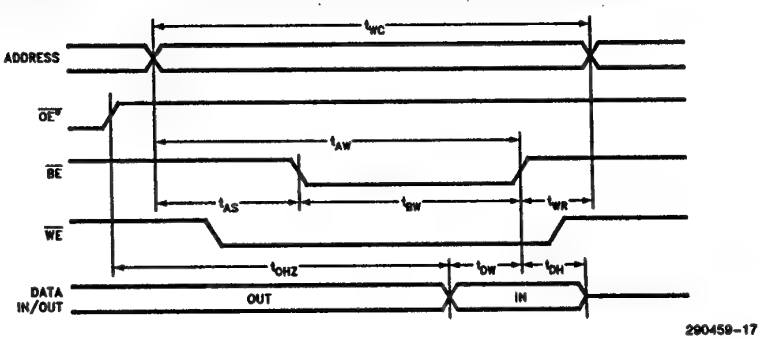
NOTES:
1. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5V on output.
2. These signals are measured with C_L = 5 pF.
3. Does not apply for separate data in and data out buses.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled Timing)



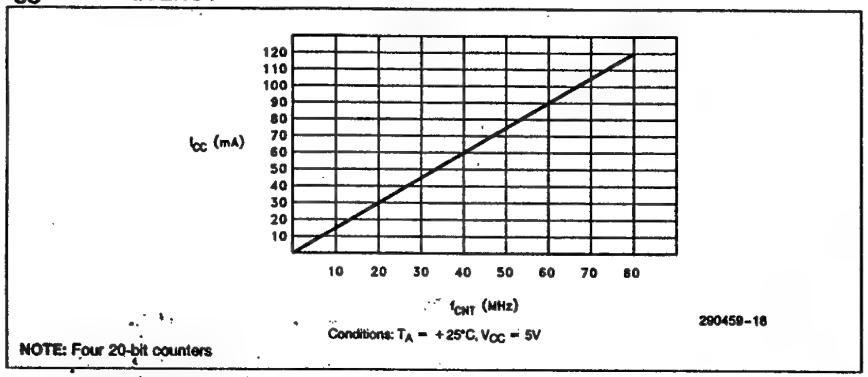
NOTE:
Cycle shown is for common data in and data out bus.

TIMING WAVEFORM OF WRITE CYCLE #2 ($\overline{BE}$ Controlled Timing)



NOTE:
Cycle shown is for common data in and data out bus.

I_{CC} vs FREQUENCY



NOTE: Four 20-bit counters

POWER-UP RESET

Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic. The power-up cycle is complete within a delay of t_{PR} after V_{CC} reaches the V_{ON} value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state.

POWER-UP RESET CHARACTERISTICS

Symbol	Parameter	Value
t_{PR}	Power-Up Reset Time	100 µs Max
V_{ON}	Turn-On Voltage	4.75V Min

2

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

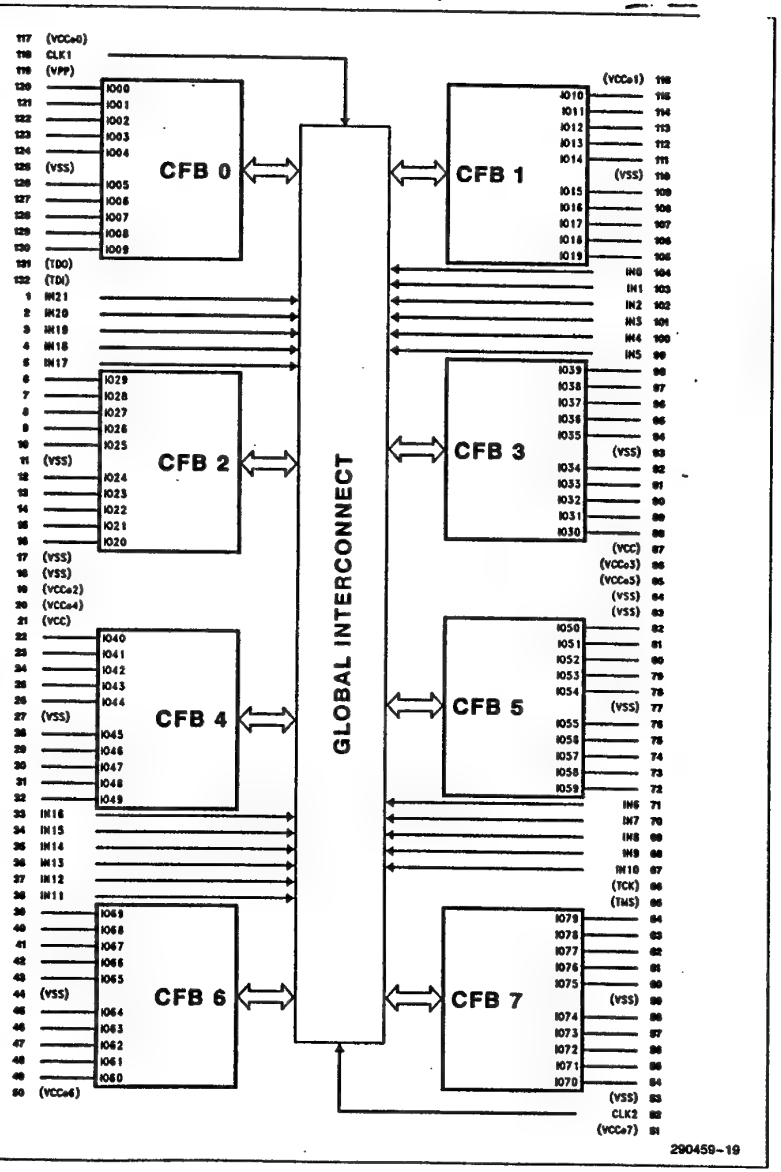
Pin Name	Description
V_{CC}	Supply voltage for the iFX780. All must be connected to 5V.
V_{SS}	Ground connections for the iFX780. All must be connected to GND.
V_{PP}	Programming voltage for the iFX780. During programming, 12.75V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC} or GND.
INx	Input only pins. These pins may not be available on all packages.
TDI	The Testability Data Input is the boundary scan serial data input to the iFX780. JTAG instructions and data are shifted into the iFX780 on the TDI input pin on the rising edge of TCK.
TDO	The Testability Data Output is the boundary scan serial data output from the iFX780. JTAG instructions and data are shifted out of the iFX780 on the TDO output on the falling edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the iFX780. TCK is used to clock state information and data into and out of the iFX780 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 20 MHz.
TMS	The Testability Control input is the boundary scan test mode select for the iFX780.

Table 5 lists the user defined pin names and descriptions.

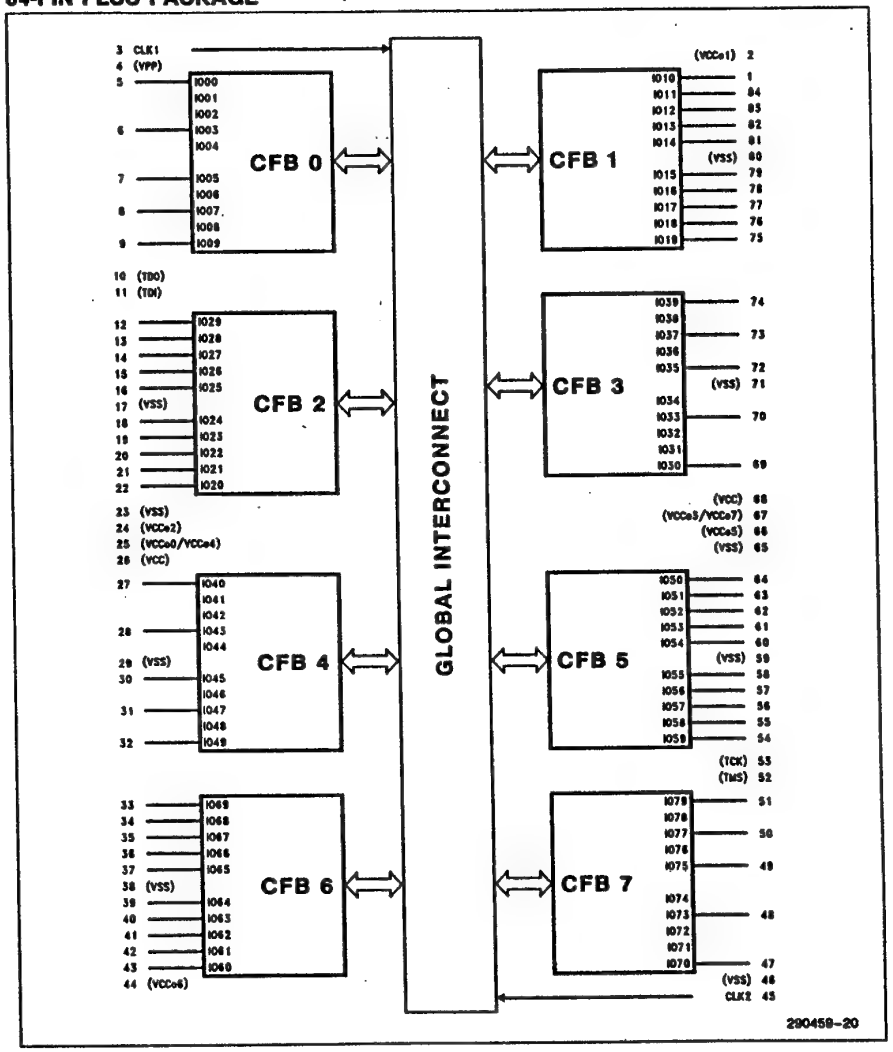
Table 5. User-Defined Pins

Pin Name	Description
V_{CCOx}	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals.
CLKx	Global clocks.
I/Oxx	Pins that can be configured either as an input or an output.

132-PIN PQFP PACKAGE



84-PIN PLCC PACKAGE



FPGA Tutorial

Electronic design has been a process of defining and implementing "black boxes". System level parameters are defined, and the system black box is broken into subsystem black boxes, which are subdivided again and again until the component level is reached. FPGAs were developed to function as large, highly-integrated black boxes to implement diverse logic functions, and the FLEXlogic FPGA family gives a designer the ultimate, flexible black box.

FLEXlogic FPGAs were designed to meet increasingly stringent design requirements. The first members of the FLEXlogic family can operate at 80 MHz system frequencies with predictable 10 ns pin-to-pin logic delays. FLEXlogic FPGAs are designed with Configurable Function Blocks (CFB) that can function as 24V10-like logic or SRAM. The CFBs are interconnected with Intel's high-speed Global Interconnect Matrix that allows PLD-like performance in a high density device. Besides traditional sum-of-products and register logic functions, FLEXlogic CFBs can also perform fast identity compares or be configured as a block of 128 x 10 SRAM.

You can start developing with FLEXlogic now using Intel's free PLDshell Plus development tool. This tutorial will show you how to create a simple design using PLDshell Plus. You can also create FLEXlogic designs using the development tools that you now use; FLEXlogic FPGAs are supported on most third-party development tool systems.

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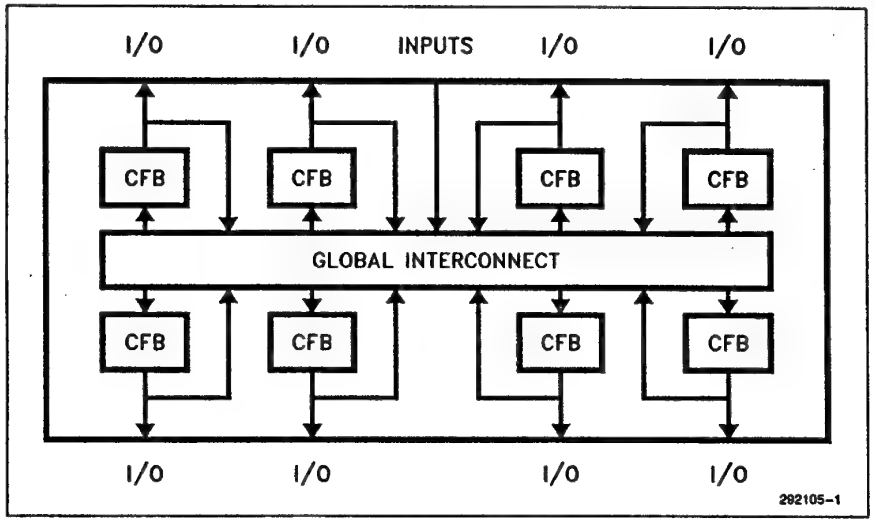


Figure 1. IFX780 Block Diagram

Order Number: 292105-001

Designing with FLEXlogic

FLEXlogic™ FPGAs are as easy to design with as the earliest PLDs; simply write the logical equations, develop a truth table, or enter the schematic equivalent.

$$out1 = in1 * in3 + in4 * in5 * in6 * in7 * in8 * in9 * in10$$

Up to 16 product terms can be included in a single sum-of-products equation. Most functions require three or fewer product terms, but some functions require many more product terms to implement. Giving each macrocell enough resources to implement all functions is wasteful and expensive, but macrocells must also be able to implement large, complex functions. FLEXlogic™ uses an innovative product-term allocation scheme to maximize resource utilization and design fit. Pairs of product terms are steered from one macrocell to its neighbor, allowing macrocells to implement functions with up to 16 product terms.

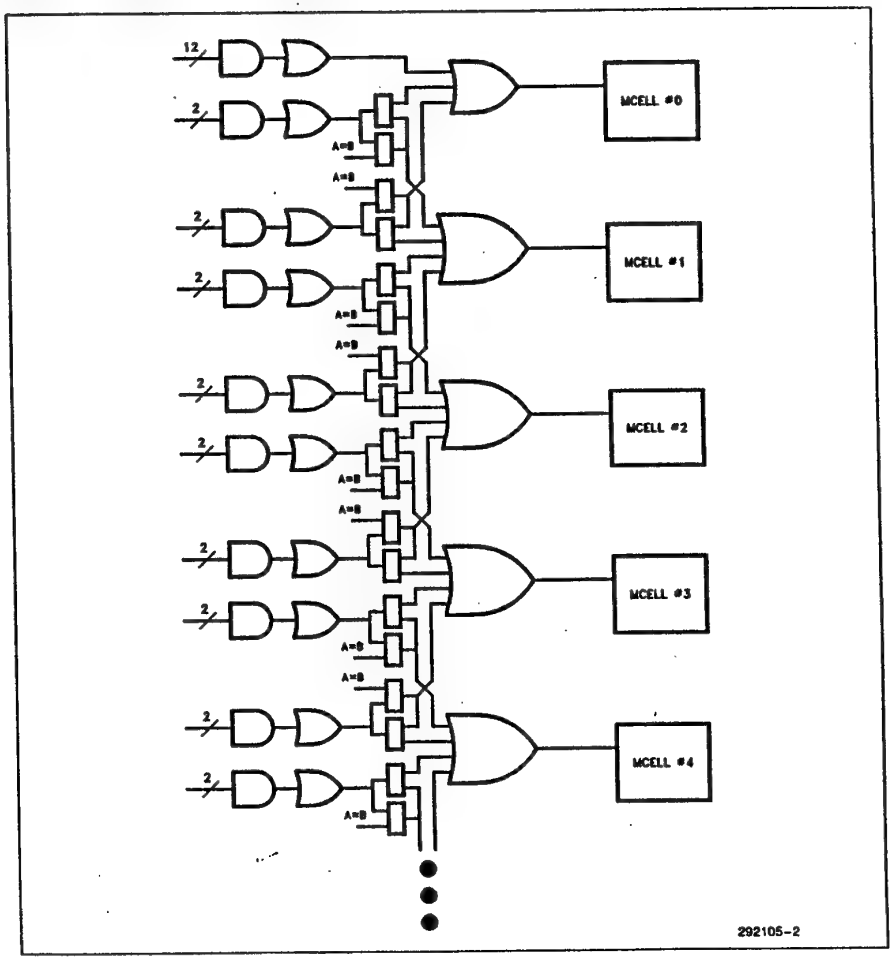


Figure 2. Product Term Allocation

Identity Compare

Identity compares can be defined in parallel with other logic functions:

out2.CMP = [C[0:11]] == [D]0:11]]

The comparator uses the same inputs as other CFB logic, and works in parallel, so that compares can be included in logic equations, and still deliver the result in 10 ns.

Timing

Determining if FLEXlogic can meet your timing requirements is equally easy; all combinatorial functions requiring one pass through a Configurable Function Block take 10 ns. This includes 16 product-term equations and 12-bit identity compares.

Function results can be loaded into macrocell registers. Each register can be individually configured as a D or T register. SR and JK registers can also be emulated. Register clocking is user programmable in each macrocell, accommodating a variety of timing requirements. Registers can be clocked on the rising or falling edge of an external clock, a delayed external clock, or a function generated clock.

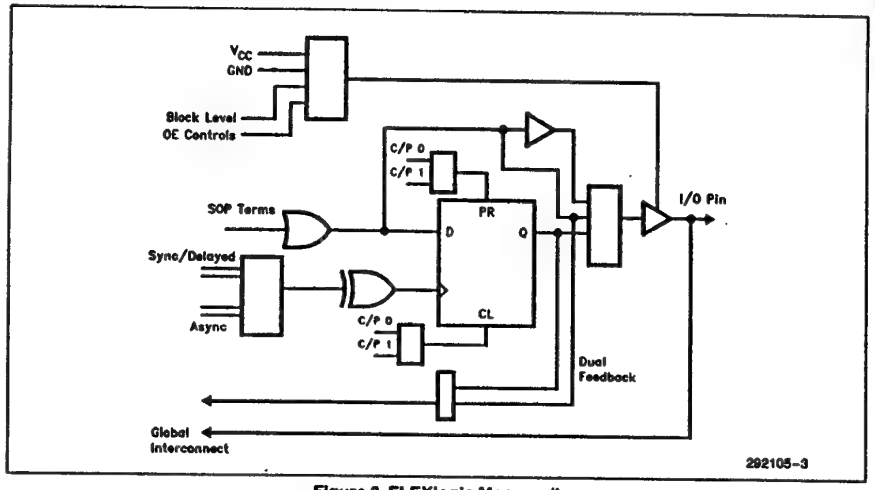


Figure 3. FLEXlogic Macrocell

```
PIN  clk1                  ;define a synchronous clock
out1.CLKF = clk1           ;clock on rising edge
out2.CLKF = /clk1          ;clock on falling edge
out3.CLKF = clk1 DELAYCLK  ;delayed clock
out4.CLKF = in8*in3*in4    ;function generated clock
```

The result, either registered or combinatorial, of each macrocell is always feedback to the Global Interconnect Matrix. The macrocell's I/O pin can be an output, input, or bi-directional, and is always available to the Global Interconnect Matrix.

```
out1.TRST = VCC            ;dedicated output
out2.TRST = GND            ;dedicated input
out3.TRST = in1*in2        ;bi-directional
```


CFB as SRAM

Each CFB can be independently configured as 15 ns SRAM.

```
PIN BUFFRAM[0:9]      RAM

BUFFRAM[0:6].ADDR = A0, A1, A2, A3, A4, A5, A6
BUFFRAM[0:9].DATA = DIN[0:9]
BUFFRAM.BE = in8
BUFFRAM.WE = write_enable
```

3.3V/5V I/O

The physical limitations of silicon demand that high-performance electrical designs move to 3.3V or lower voltages. FLEXlogic FPGAs are the first programmable logic devices to address designers' needs for 3.3V and 5V logic. Each CFB can be configured as 3.3V or 5V logic by tying its V_{CCO} pin to the appropriate supply voltage. Adding 3VOLT or 5VOLT to a macrocell's pin definition allows the compiler to group it with other cells with the same logic level.

```
PIN 12 OUT1 3VOLT  ;3.3V pin
```

CFB as SRAM

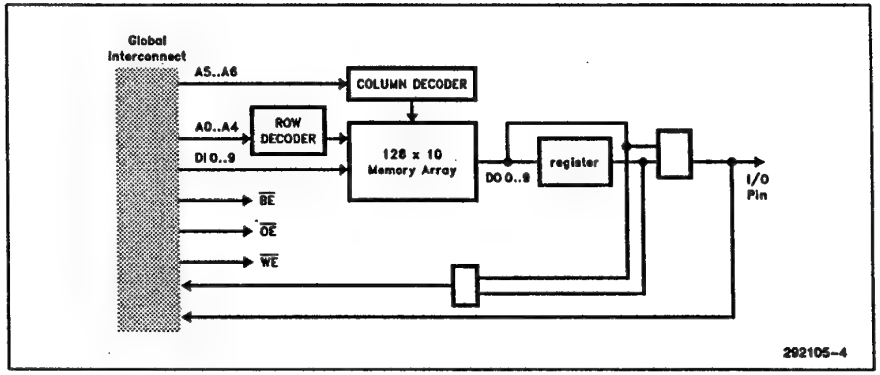


Figure 4. CFB as SRAM

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/93

MAXIM

Precision, Quad, SPDT, CMOS Analog Switch

General Description

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±4.5V to ±20V, or with a single-ended supply between +10V and +30V. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than 1µA with all inputs high or low.

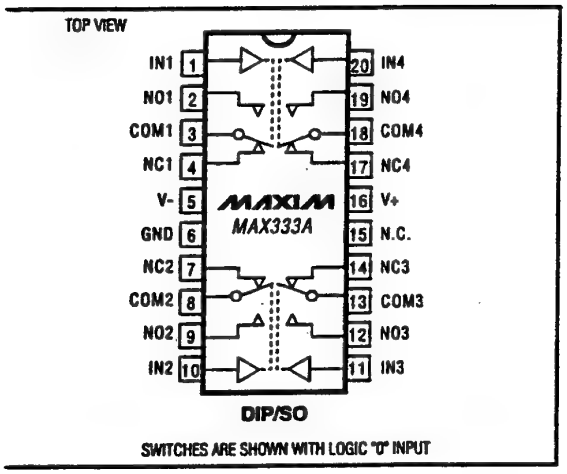
This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35µW), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL- and CMOS-compatible and guaranteed over a +0.8V to +2.4V range, regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage. This upgraded part is a replacement for a DG211/DG212 pair when used as a quad SPDT switch, or two DG403 dual SPDT switches.

Applications

Test Equipment
Communications Systems
PBX, PABX
Heads-Up Displays
Portable Instruments

Pin Configuration



Features

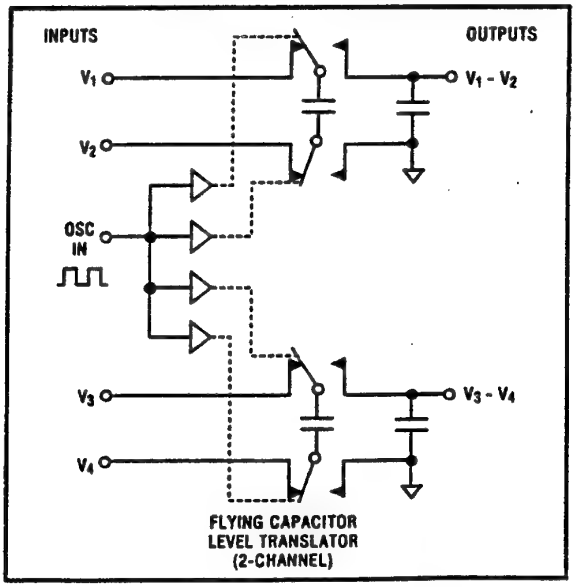
- ♦ **Upgraded Replacement for a DG211/DG212 Pair or Two DG403s**
- ♦ Low On Resistance < 22Ω Typical (35Ω Max)
- ♦ **Guaranteed Matched On Resistance Between Channels < 2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection < 10pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ ESD Guaranteed > 2000V per Method 3015.7
- ♦ Single-Supply Operation (+10V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ TTL-/CMOS-Logic Compatibility
- ♦ Rail-to-Rail Analog Signal Handling Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX333ACPP	0°C to +70°C	20 Plastic DIP
MAX333ACWP	0°C to +70°C	20 Wide SO
MAX333AC/D	0°C to +70°C	Dice*
MAX333AEPP	-40°C to +85°C	20 Plastic DIP
MAX333AEWP	-40°C to +85°C	20 Wide SO
MAX333AMJP	-55°C to +125°C	20 CERDIP

* *Contact factory for dice specifications.*

Typical Operating Circuit



DG444/445
Monolithic Quad SPST CMOS Analog Switches

Siliconix incorporated

FEATURES

- ±15 Volt Input Range
- ON Resistance < 80 Ω
- Fast Switching Action
  t_{ON} < 160 ns
  t_{OFF} < 80 ns
- TTL, CMOS Compatible
- DG211/DG212 Upgrades
- ESDS Protection > ±4000 V

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Simple Interfacing

APPLICATIONS

- Sample and Hold circuits
- Data Acquisition
- Automatic Test Equipment
- Audio and Video Switching
- Communication Systems
- Battery Operated Systems

DESCRIPTION

The DG444 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog signals. Combining low power (< 35 microwatts) with high speed (t_{ON} < 160 ns), the DG444/445 is ideally suited for upgrading DG211/DG212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444 series was built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range limitation.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. Packaging options include the 16-pin plastic and small outline. The performance grade for this series is the industrial, D suffix (–40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG444

Four SPST Switches per Package

Truth Table

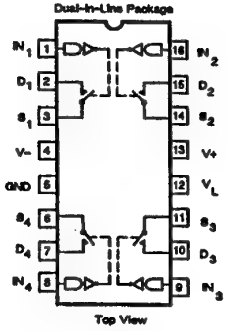
LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

SO Package

Top View
Order Number: DG444DY

Dual-In-Line Package



Top View
Order Numbers: DG444DJ

Preliminary

FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION

DG445

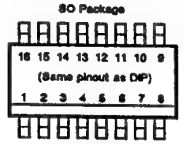
Four SPST Switches per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

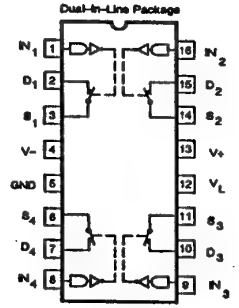
Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

SO Package



Top View
Order Number: DG445DY

Dual-In-Line Package



Top View
Order Numbers: DG445DJ

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–
V+ ..... 44 V
GND ..... 25 V
V_L ..... (GND –0.3 V) to 44 V
Digital Inputs V_S,V_D[1] ... (V– minus 2 V) to (V+ plus 2 V)
..... or 30 mA, whichever occurs first
Current (Any Terminal) continuous ..... 30 mA
Current (S or D) Pulsed 1 ms, 10% duty ..... 100 mA
Storage Temperature (D Suffix) ..... –65 to 125°C
Operating Temperature (D Suffix) ..... –40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin SO*** ..... 600 mW

* All leads welded or soldered to PC Board.
** Derate 6 mW/°C above 75°C.
*** Derate 7.6 mW/°C above 75°C.
1 Signals on Sx, Dx, or INx exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V– = –15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4, 0.8 V[e]	LIMITS 1=25°C 2=85°C 3=–40°C TEMP	TYP[d]	D SUFFIX –40 to 85°C MIN[b]	MAX[b]	UNIT
SWITCH							
Analog Signal Range[e]	V_{ANALOG}				–15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = –10 mA, V_D = ±8.5 V, V+ = 13.5 V, V– = –13.5 V	1,3			80	Ω
			2			100	
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V– = –16.5 V, V_D = ±15.5 V, V_S = ±15.5 V	1		–0.25	0.25	nA
			2		–20	20	
	$I_{D(OFF)}$		1		–0.25	0.25	
			2		–20	20	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V– = –16.5 V, V_S = V_D = ±15.5 V	1		–0.4	0.4	
			2		–40	40	

Preliminary

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4, 0.8 V [e]	LIMITS 1=25°C 2=85°C 3=-40°C TEMP	TYP [d]	D SUFFIX -40 to 85°C MIN [b]	MAX [b]	UNIT
INPUT							
Input Current with V_{IN} LOW	I_{IL}	V_{IN} Under Test = 0.8 V, All Other = 2.4 V	1,2		-0.5	0.5	µA
Input Current with V_{IN} HIGH	I_{IH}	V_{IN} Under Test = 2.4 V, All Other = 0.8 V	1,2		-0.5	0.5	µA
DYNAMIC							
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 5 pF, See Figure 1, V_S = ±10 V	1			160	ns
Turn-OFF Time	t_{OFF}		1			80	ns
Charge Injection [c]	Q	C_L = 10 nF, V_S = 0 V, V_{gen} = 0 V, R_{gen} = 0 Ω	1		-10	10	pC
SUPPLY							
Positive Supply Current	I_+	V+ = 16.5 V, V- = -16.5 V, V_{IN} = 0 or 5 V	1 2			1 5	µA
Negative Supply Current	I_-		1 2		-1 -5		µA
Logic Supply Current	I_L		1 2			1 5	µA
Ground Current	I_{GND}		1 2		-1 -5		µA

ELECTRICAL CHARACTERISTICS [a] (UNIPOLAR SUPPLY)

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 12 V, V- = 0 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4, 0.8 V [e]	LIMITS 1=25°C 2=85°C 3=-40°C TEMP	TYP [d]	D SUFFIX -40 to 85°C MIN [b]	MAX [b]	UNIT
SWITCH							
Analog Signal Range [c]	V_{ANALOG}				0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = 3 V, 8 V, V+ = 10.8 V, V_L = 5.25 V	1 2,3			160 200	Ω

ELECTRICAL CHARACTERISTICS [a] (UNIPOLAR SUPPLY)

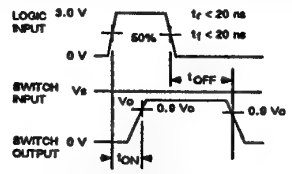
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 12 V, V- = 0 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4, 0.8 V [e]	LIMITS 1=25°C 2=85°C 3=-40°C TEMP	TYP [d]	D SUFFIX -40 to 85°C MIN [b]	MAX [b]	UNIT
DYNAMIC							
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 1, V_S = 8 V	1			400	ns
Turn-OFF Time	t_{OFF}		1			200	ns
Charge Injection [c]	Q	C_L = 10 nF, V_L = 5.25 V, V_{gen} = 6.6 V, R_{gen} = 0 Ω, V+ = 13.2 V	1		-40	40	pC
SUPPLY							
Positive Supply Current	I_+	V+ = 13.2 V, V_{IN} = 0 or 5 V	1 2,3			1 5	µA
Negative Supply Current	I_-	V_{IN} = 0 or 5 V	1 2,3		-1 -5		µA
Logic Supply Current	I_L	V_L = 5.25 V, V_{IN} = 0 or 5 V	1 2,3			1 5	µA
Ground Current	I_{GND}	V_{IN} = 0 or 5 V	1 2,3		-1 -5		µA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.

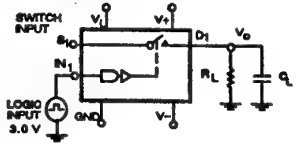
5

SWITCHING TIME TEST CIRCUIT

V_O is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense

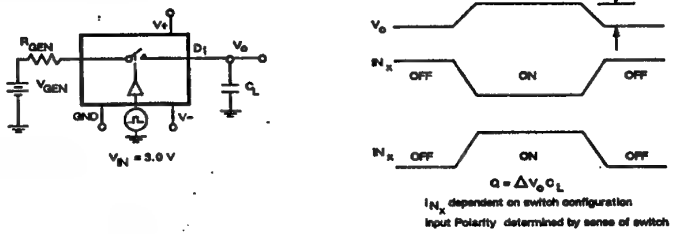


Repeat test for Ch 2, 3, 4

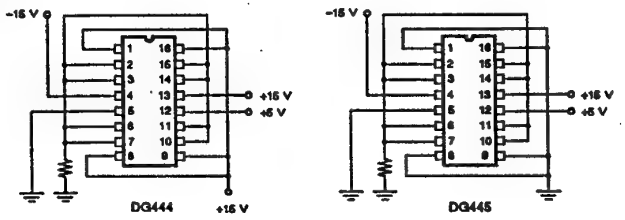
For load conditions, See Electrical Characteristics
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

CHARGE INJECTION TEST CIRCUIT

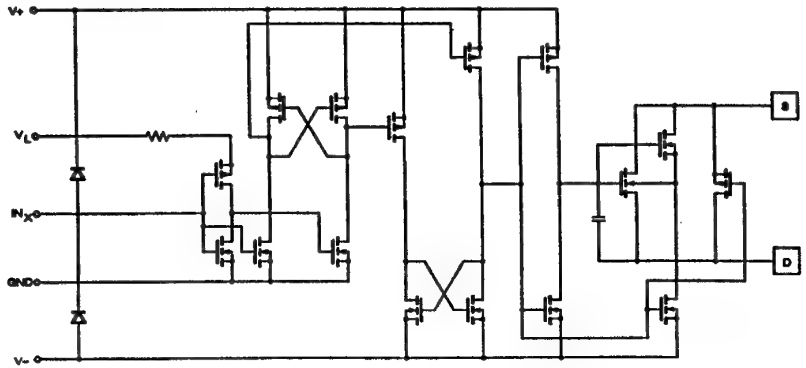


BURN-IN CIRCUITS

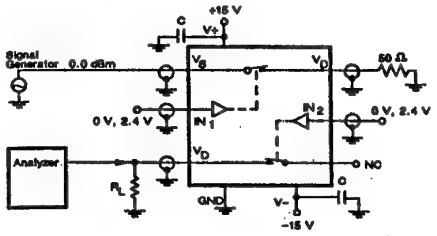


Note: All Resistors are 10 kΩ unless otherwise specified

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

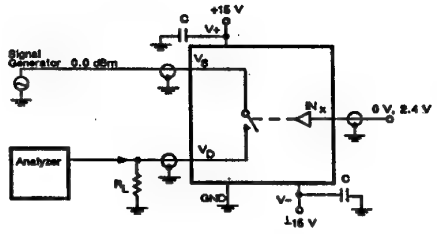


CROSSTALK TEST CIRCUIT



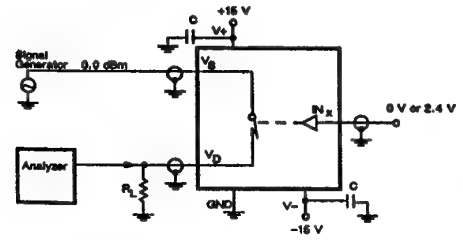
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

OFF ISOLATION TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

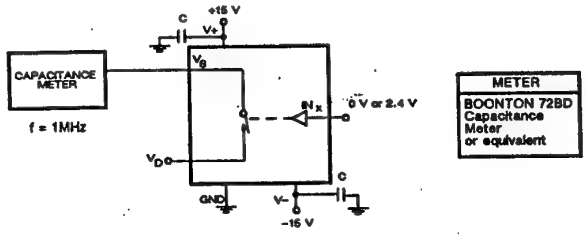
INSERTION LOSS TEST CIRCUIT



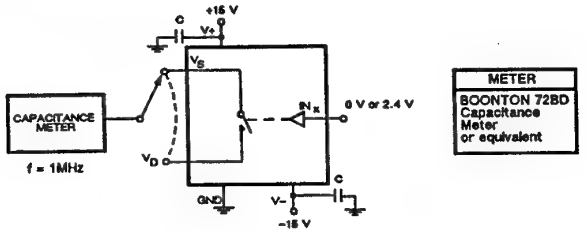
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

5

SOURCE + DRAIN ON CAPACITANCE



SOURCE + DRAIN OFF CAPACITANCE



PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	Analog Channel Input or Output
D	Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V–	Negative Supply Voltage
GND	Digital Ground
V_L	Logic Supply Voltage

APPLICATIONS

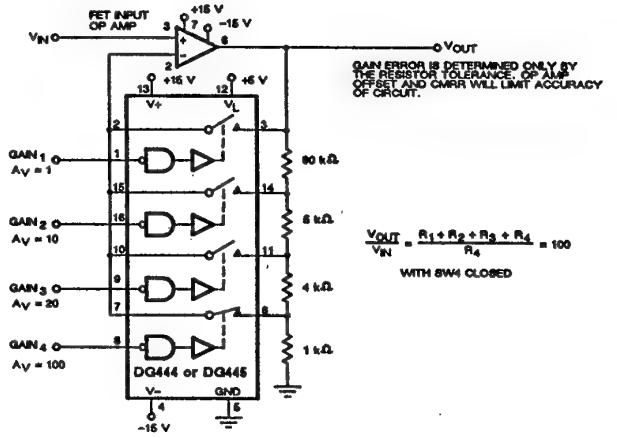


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

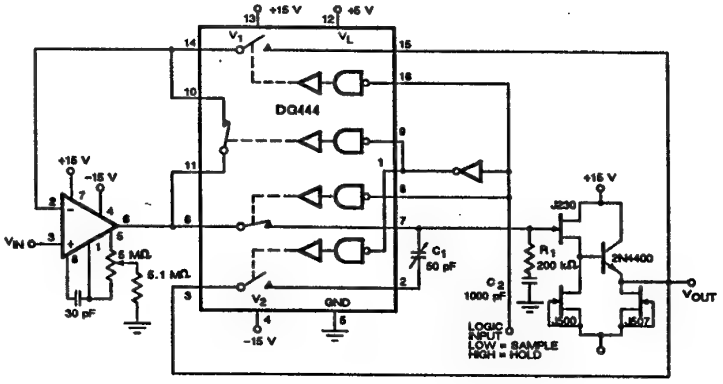


Figure 7. Precision Sample-and-Hold

BURR-BROWN®

OPA627
OPA637

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: 4.5nV/√Hz at 10kHz
- FAST SETTLING TIME:
  OPA627—550ns to 0.01%
  OPA637—450ns to 0.01%
- LOW V_{OS}: 100µV max
- LOW DRIFT: 0.8µV/°C max
- LOW I_B: 5pA max
- OPA627: Unity-Gain Stable
- OPA637: STABLE IN GAIN ≥5

APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

DESCRIPTION

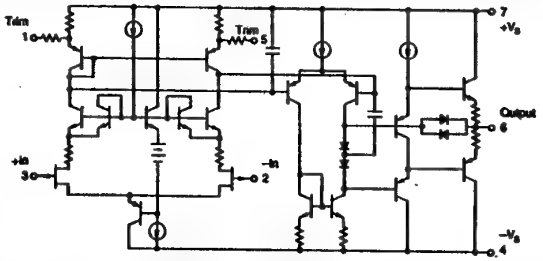
The OPA627 and OPA637 *Difet* operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage—±4.5V to ±18V. Laser-trimmed *Difet* input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-998B

SPECIFICATIONS

ELECTRICAL

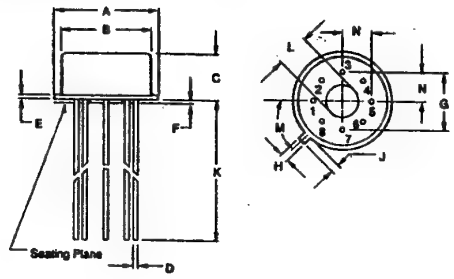
T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	OPA627BM/BP/SM OPA637BM/BP/SM MIN	TYP	MAX	OPA627AM/AP/AU OPA637AM/AP/AU MIN	TYP	MAX	UNITS
OFFSET VOLTAGE [1]								
Input Offset Voltage								
AP, BP, AU Grades			40	100		130	250	µV
Average Drift			100	250		280	500	µV
AP, BP, AU Grades			0.4	0.8		1.2	2	µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106	0.8 120	2	100	2.5 116		µV/°C dB
INPUT BIAS CURRENT [2]								
Input Bias Current	V_{CM} = 0V		1	5		2	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade	V_{CM} = 0V			50				nA
Over Common-Mode Voltage	V_{CM} = ±10V		1			2		pA
Input Offset Current	V_{CM} = 0V		0.5	5		1	10	pA
Over Specified Temperature	V_{CM} = 0V			1			2	nA
SM Grade				50				nA
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.8		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1 to 10Hz			0.8	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 1kHz			1.8	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1 to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{10} ‖ 6			•		Ω ‖ pF
Common-Mode			10^{13} ‖ 7			•		Ω ‖ pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±11	±11.5		•	•		V
Over Specified Temperature		±10.5	±11		•	•		V
Common-Mode Rejection	V_{CM} = ±10.5V	106	116		100	110		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	112	120		106	116		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	106	117		100	110		dB
SM Grade	V_O = ±10V, R_L = 1kΩ	100	114					dB
FREQUENCY RESPONSE								
Slew Rate: OPA627	G = −1, 10V Step	40	55		•	•		V/µs
OPA637	G = −4, 10V Step	100	135		•	•		V/µs
Settling Time: OPA627 0.01%	G = −1, 10V Step		550			•		ns
0.1%	G = −1, 10V Step		450			•		ns
OPA637 0.01%	G = −4, 10V Step		450			•		ns
0.1%	G = −4, 10V Step		300			•		ns
Gain-Bandwidth Product: OPA627	G = 1		16			•		MHz
OPA637	G = 10		80			•		MHz
Total Harmonic Distortion + Noise	G = +1, f = 1kHz		0.00003			•		%
POWER SUPPLY								
Specified Operating Voltage			±15			•		V
Operating Voltage Range		±4.5		±18	•		•	V
Current			±7	±7.5		•	•	mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±11.5	±12.3		•	•		
Over Specified Temperature		±11	±11.5		•	•		V
Current Output	V_O = ±10V		±45			•		mA
Short Circuit Current		±35	+70/−65	±100	•	•	•	mA
Output Impedance, Open-Loop	1MHz		55			•		Ω
TEMPERATURE RANGE								
Specification: AP, BP, AM, BM, AU		−25		+85	•		•	°C
SM		−55		+125				°C
Storage: AM, BM, SM		−60		+150	•		•	°C
AP, BP, AU		−40		+125	•		•	°C
θ_{JA}: AM, BM, SM			200			•		°C/W
AP, BP, AU			100			•		°C/W

* Specifications same as OPA627B grade.
NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = 25°C. See Typical Performance Curves for warmed-up performance.

MECHANICAL

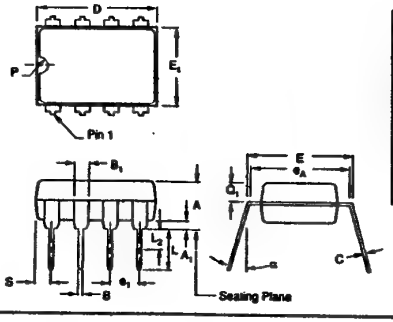
M Package — Metal TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP



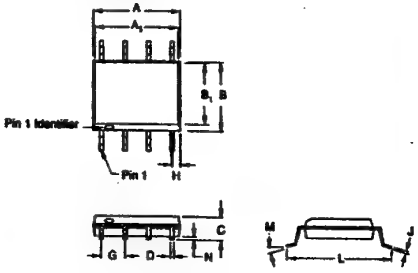
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.200	3.94	5.08
A1	.020	.050	0.51	1.27
B	.014	.020	0.36	0.51
B1	.045	.065	1.14	1.65
C	.008	.012	0.20	0.30
D(1)	.370	.400	9.40	10.16
E	.300	.325	7.62	8.26
E1	.240	.260	6.10	6.60
e1	.100 BASIC		2.54 BASIC	
eA	.300 BASIC		7.62 BASIC	
L	.125	.150	3.18	3.81

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L2(2)	0	.030	0.00	0.76
α	0°	15°	0°	15°
P	.015	.050	0.38	1.270
Q1	.040	.075	1.02	1.91
S1(2)	.015	.050	0.38	1.27

(1) Not JEDEC Std.
(2) e1 and eA applies in zone L2 when unit located.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

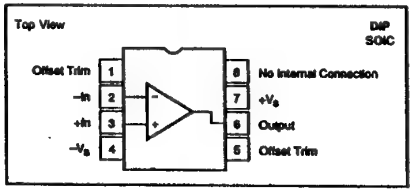
U Package — 8-Pin SOIC

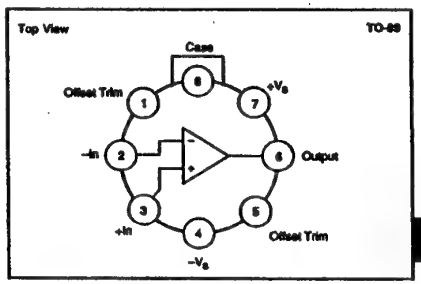


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.148	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.68
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

PIN CONFIGURATIONS





ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	–25°C to +85°C
OPA627BP	Plastic DIP	–25°C to +85°C
OPA627AU	SOIC	–25°C to +85°C
OPA627AM	TO-99 Metal	–25°C to +85°C
OPA627BM	TO-99 Metal	–25°C to +85°C
OPA627SM	TO-99 Metal	–55°C to +125°C
OPA637AP	Plastic DIP	–25°C to +85°C
OPA637BP	Plastic DIP	–25°C to +85°C
OPA637AU	SOIC	–25°C to +85°C
OPA637AM	TO-99 Metal	–25°C to +85°C
OPA637BM	TO-99 Metal	–25°C to +85°C
OPA637SM	TO-99 Metal	–55°C to +125°C

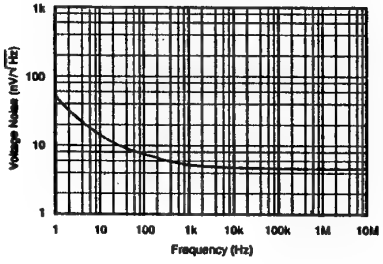
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$+V_S$ + 2V to $-V_S$ – 2V
Differential Input Range	Total V_S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	–55°C to +150°C
P, U Package	–40°C to +125°C
Storage Temperature	
M Package	–55°C to +150°C
P, U Package	–40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

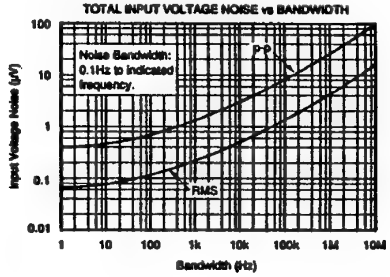
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

INPUT VOLTAGE NOISE SPECTRAL DENSITY



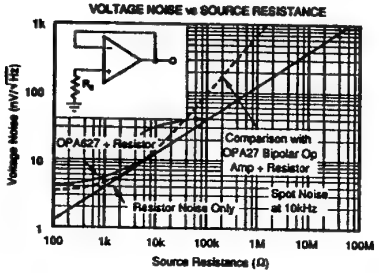
TOTAL INPUT VOLTAGE NOISE vs BANDWIDTH



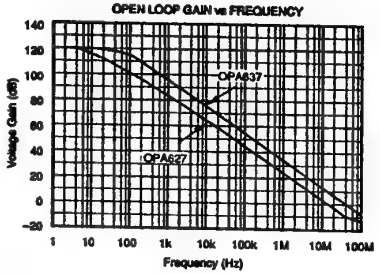
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

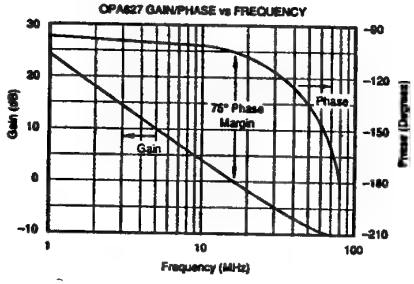
VOLTAGE NOISE vs SOURCE RESISTANCE



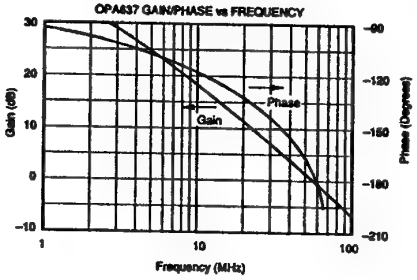
OPEN LOOP GAIN vs FREQUENCY



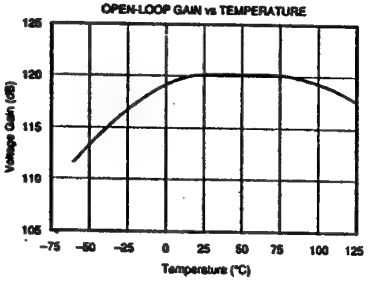
OPA627 GAIN/PHASE vs FREQUENCY



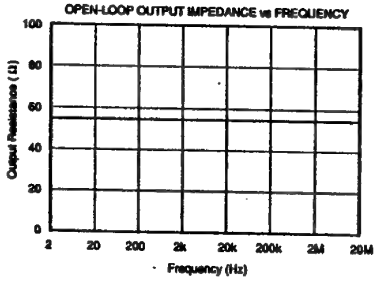
OPA637 GAIN/PHASE vs FREQUENCY



OPEN-LOOP GAIN vs TEMPERATURE



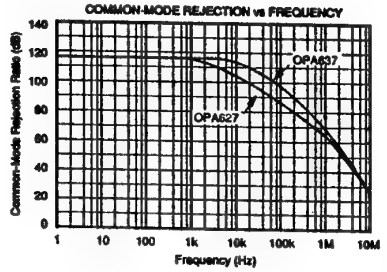
OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



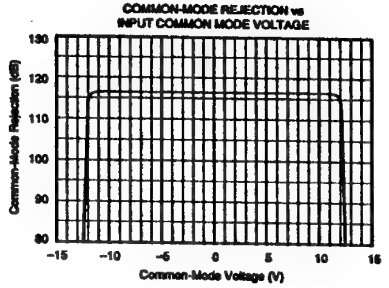
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

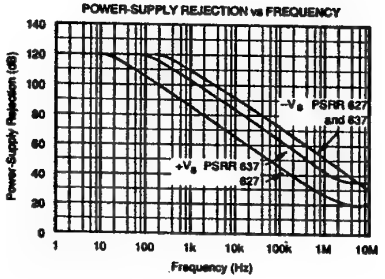
COMMON-MODE REJECTION vs FREQUENCY



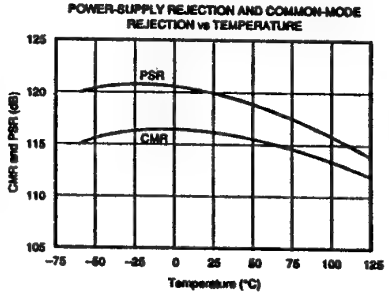
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



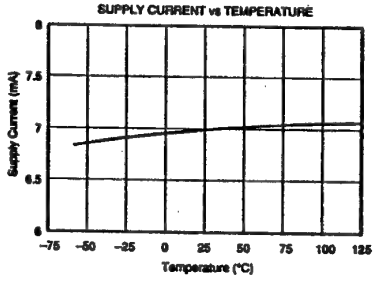
POWER-SUPPLY REJECTION vs FREQUENCY



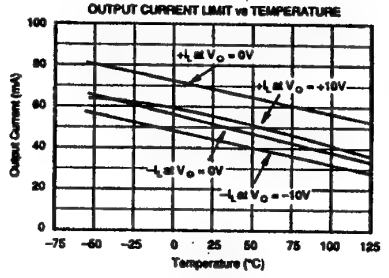
POWER-SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



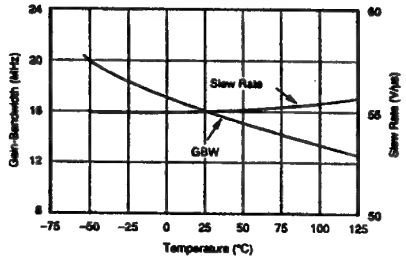
OUTPUT CURRENT LIMIT vs TEMPERATURE



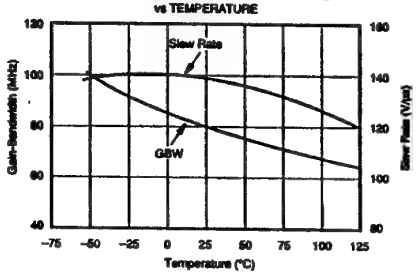
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

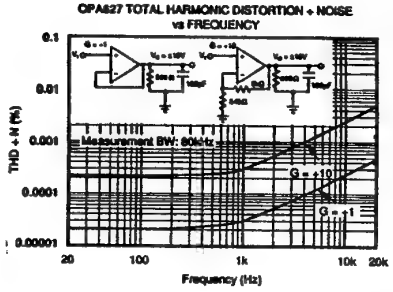
OPA627 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



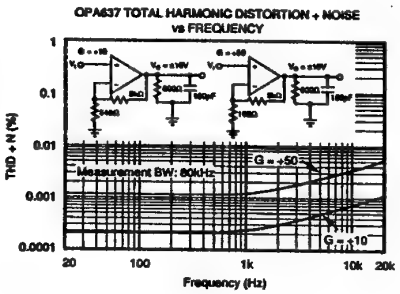
OPA637 GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



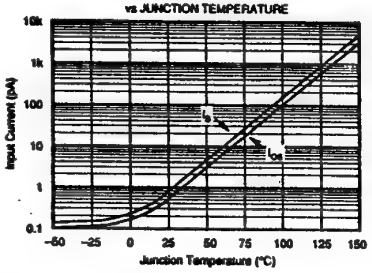
OPA627 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



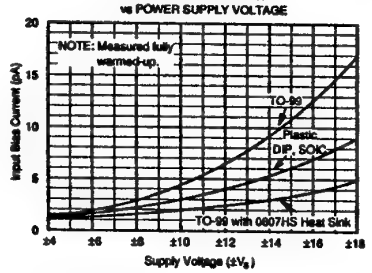
OPA637 TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



INPUT BIAS AND OFFSET CURRENT vs JUNCTION TEMPERATURE



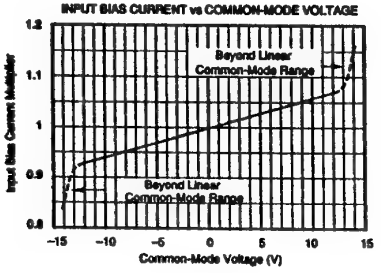
INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



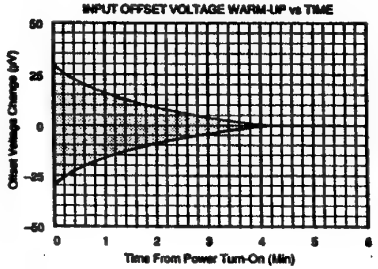
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

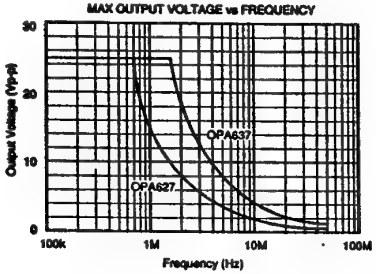
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



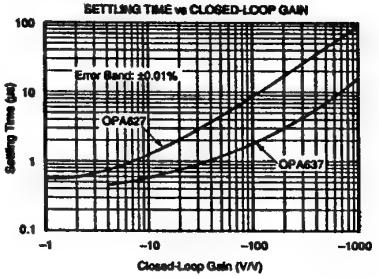
INPUT OFFSET VOLTAGE WARM-UP vs TIME



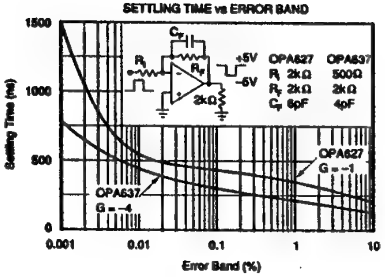
MAX OUTPUT VOLTAGE vs FREQUENCY



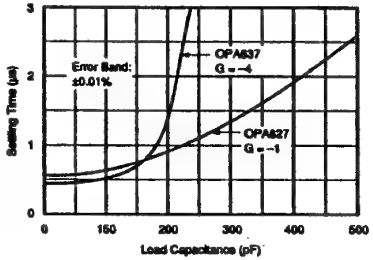
SETTLING TIME vs CLOSED-LOOP GAIN



SETTLING TIME vs ERROR BAND



SETTLING TIME vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

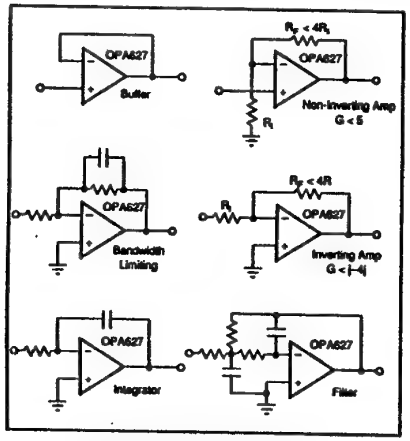


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

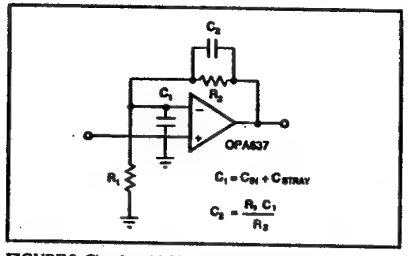


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift.

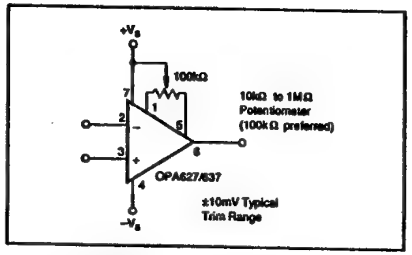


FIGURE 3. Optional Offset Voltage Trim Circuit.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Above a 2kΩ source resistance, the op amp contributes little additional noise. Below 1kΩ, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal package only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

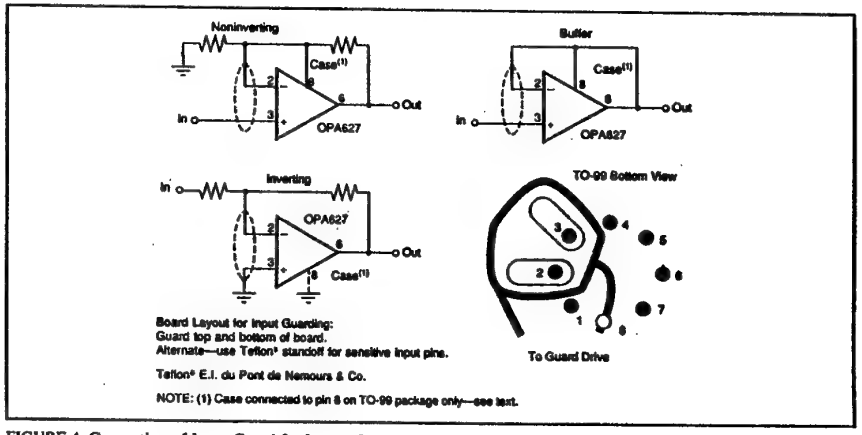


FIGURE 4. Connection of Input Guard for Lowest I_B.

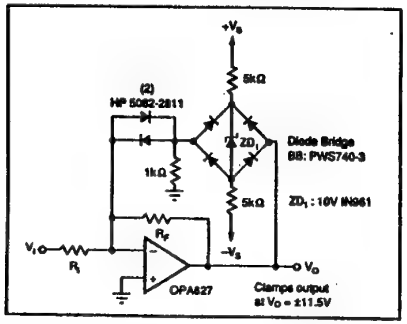


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_s + 2V$ and $-V_s - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_s, to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a $1k\Omega$ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

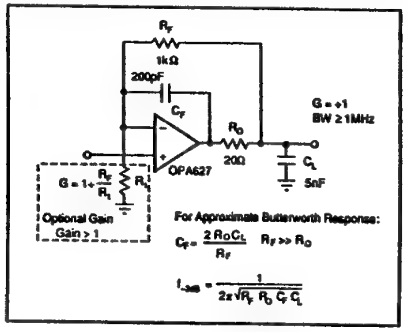


FIGURE 6. Driving Large Capacitive Loads.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

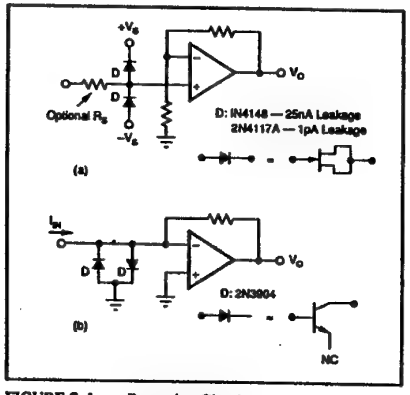


FIGURE 7. Input Protection Circuits.

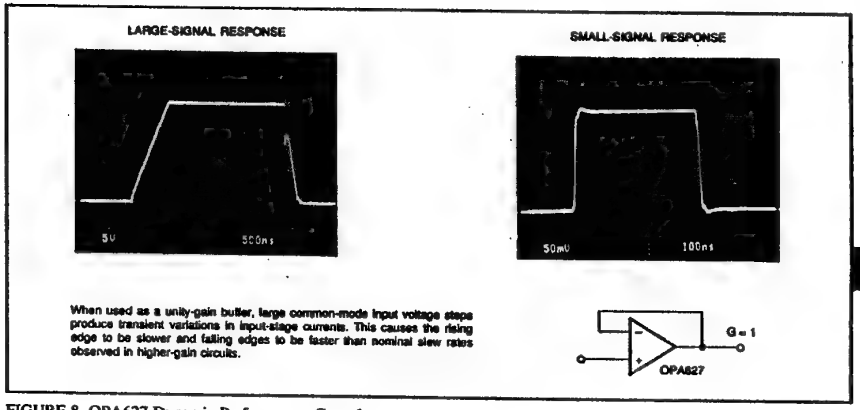


FIGURE 8. OPA627 Dynamic Performance, G = +1.

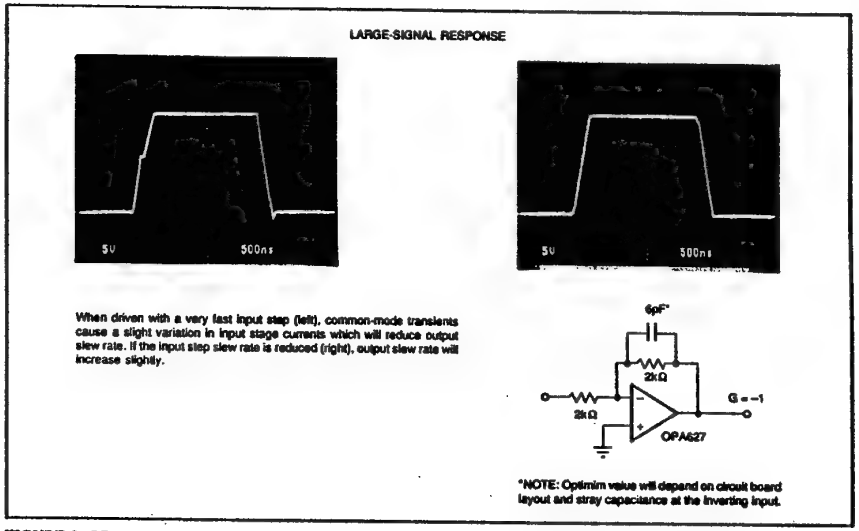


FIGURE 9. OPA627 Dynamic Performance, G = –1.

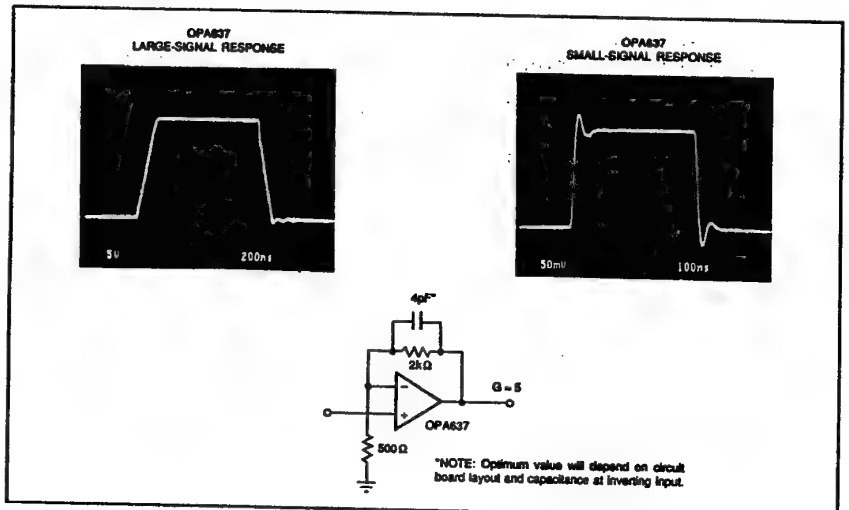


FIGURE 10. OPA637 Dynamic Response, G = 5.

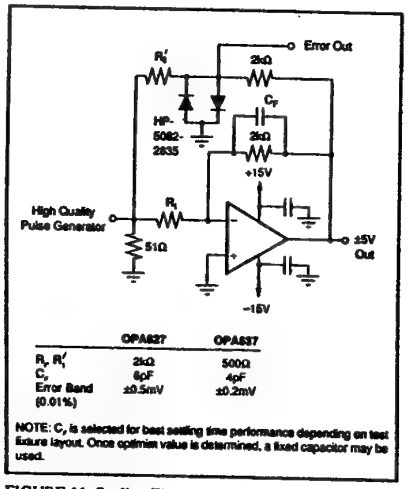


FIGURE 11. Settling Time and Slew Rate Test Circuit.

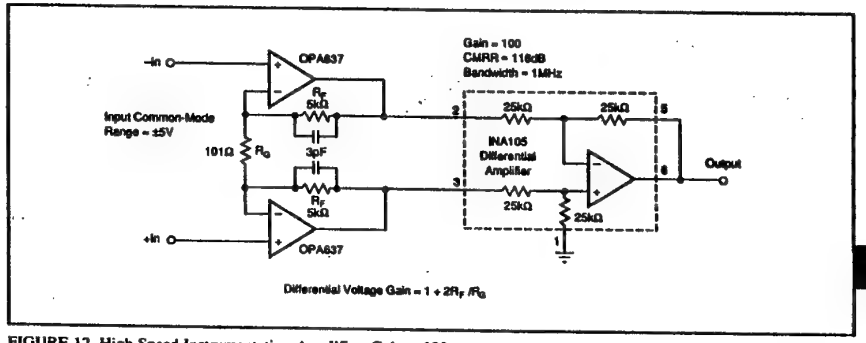


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

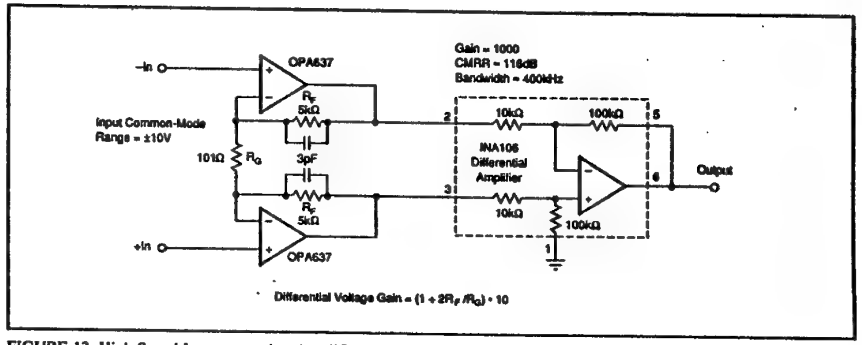
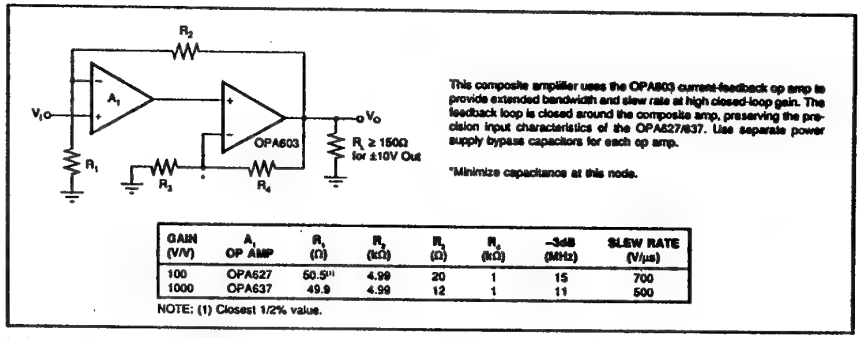


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.



GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	-3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5[1]	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 14. Composite Amplifier for Wide Bandwidth.

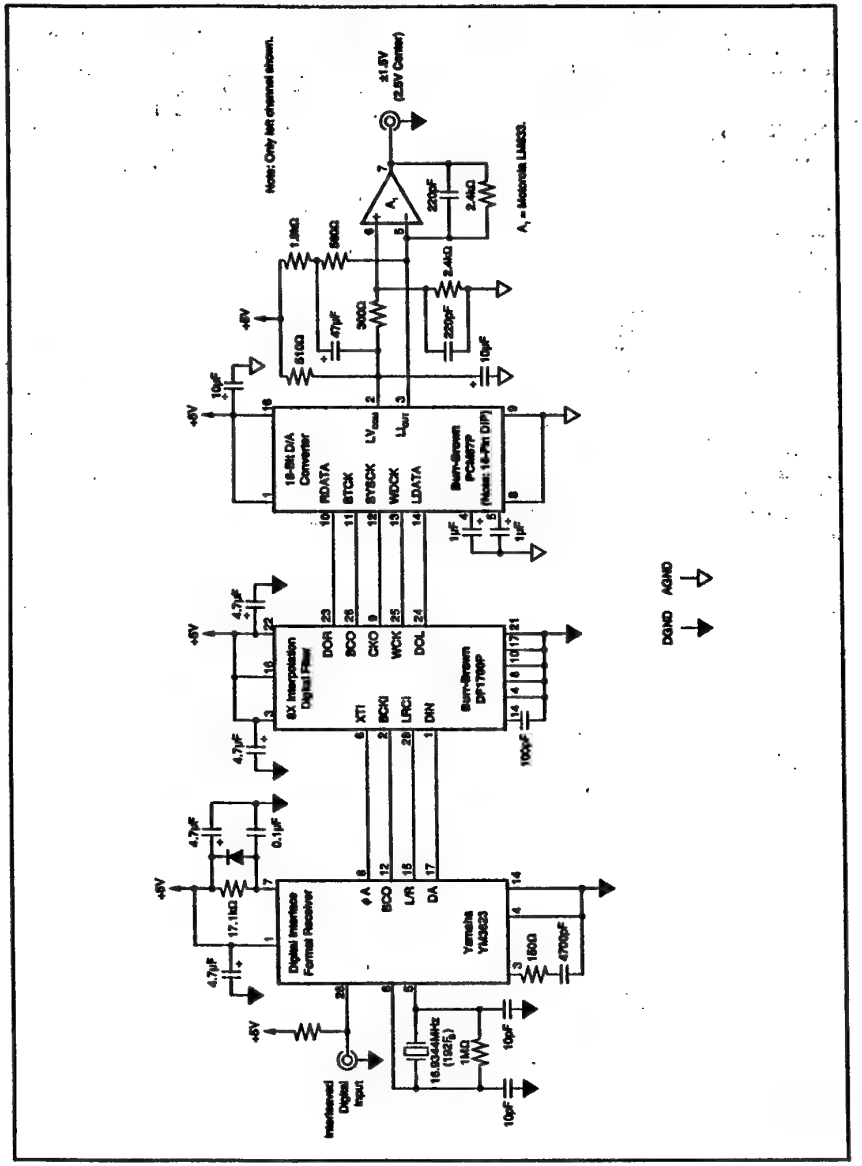
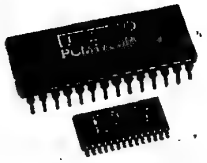


FIGURE 7. Stereo Audio Application.

BURR-BROWN®



PCM1750P
PCM1750U

Dual CMOS 18-Bit Monolithic Audio ANALOG-TO-DIGITAL CONVERTER

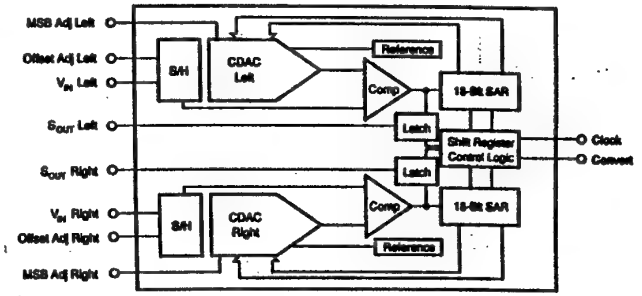
FEATURES

- DUAL 18-BIT LOW-POWER CMOS AUDIO A/D CONVERTER
- FAST 4.5µs MIN CONVERSION TIME INCLUDING S/H
- VERY LOW MAX THD+N: –88dB Without External Adjust
- COMPLETE WITH INTERNAL REFERENCE AND DUAL S/H FUNCTION
- TWO CO-PHASE SAMPLED, ±2.75V AUDIO INPUTS
- CAPABLE OF 4X PER CHANNEL OVERSAMPLING RATE
- RUNS ON ±5V SUPPLIES AND DISSIPATES 300mW MAX
- COMPACT 28-PIN PLASTIC DIP OR SOIC

DESCRIPTION

The PCM1750 is a low cost, dual 18-bit CMOS analog-to-digital converter optimized for dynamic signal applications. The PCM1750 features true co-phased inputs with an internal sample/hold function for each channel. The PCM1750 also comes complete with an internal reference. Total power dissipation is less than 300mW max using ±5V voltage supplies. Low maximum Total Harmonic Distortion + Noise (–88dB max) is 100% tested. The very fast PCM1750 is capable of 4X audio bandwidth oversampling rates on both input channels simultaneously, providing greater freedom to designers in selecting input anti-aliasing filters.

PCM1750 outputs serial data in a format that is compatible with many digital filter chips and comes packaged in a space saving 28-pin plastic DIP or SOIC.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1084B

SPECIFICATIONS

ELECTRICAL

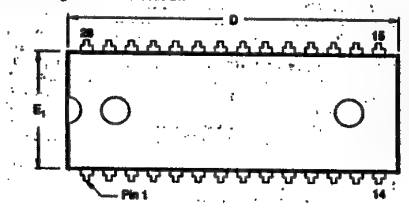
At 25°C, and $\pm V_A = \pm 5.0V$; $+V_D = +5.0V$, unless otherwise noted. Where relevant, specifications apply to both left and right input/output channels.

PARAMETER	CONDITIONS	PCM1750P/U MIN	PCM1750P/U TYP	PCM1750P/U MAX	UNITS
RESOLUTION		16			Bits
DYNAMIC RANGE	THD + N at –60dB Referred to Full Scale	+88	+90		dB
ANALOG INPUT					
Input Range			±2.75		V
Input Capacitance			20		pF
Aperture Delay			10		ns
Aperture Uncertainty (Jitter)			50		ps$_{rms}$
Full Power Input Bandwidth			500		kHz
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS Compatible		
Logic Level: V_{IH}	I_{IH} = ±5µA	+3.5		$+V_D$ + 0.3	V
V_{IL}	I_{IL} = ±5µA	–0.3		+1.5	V
V_{OH}	I_{source} = 1.0mA	+2.7	+4.7		V
V_{OL}	I_{sink} = 3.2mA		+0.2	+0.4	V
Output Data Format			Serial, MSB First, BTC[1]		
Convert Command			Positive Edge		
Convert Command Pulse Width			81		ns
Conversion Time	Throughput Including Sample/Hold[2]	4.5	5.2	20.8	µs
DYNAMIC CHARACTERISTICS (20Hz to 24kHz; 4X data decimated to 1X)					
Signal-to-Noise Ratio[3]	f_S = 192kHz[4]; f_{IN} = 1kHz (0dB)[5]	+88	+90		dB[6]
Total Harmonic Distortion + N[3]	Without External Adjustments				
f_{IN} = 1kHz (0dB)	f_S = 192kHz		–90	–86	dB
f_{IN} = 1kHz (–20dB)	f_S = 192kHz		–70	–66	dB
f_{IN} = 1kHz (–60dB)	f_S = 192kHz		–30	–26	dB
Channel Separation	f_S = 192kHz; f_{IN} = 1kHz (0dB) and 0V	+96	+108		dB
ACCURACY					
Gain Error			±2	±5	%
Gain Mismatch	Channel to Channel		±0.5	±2.0	%
BPZ (Bipolar Zero) Error[7]			±2		mV
BPZ Error Mismatch	Channel to Channel		±3		mV
BPZ Differential Linearity Error[8]			±0.002		% of FSR[6]
Linearity Error			±0.003		% of FSR
Warm-up Time			1		ms
DRIFT (With Internal Reference)					
Gain	0°C to 70°C		±50		ppm/°C
Bipolar Zero	0°C to 70°C		±10		ppm of FSR/°C
DRIFT (Exclusive of Internal Reference)					
Gain	0°C to 70°C		±10		ppm/°C
Bipolar Zero	0°C to 70°C		±3		ppm of FSR/°C
REFERENCE					
V_{REF} Output (Pins 18, 24):					
Voltage			+2.75		V
Current			±100		µA
Impedance			0.2		Ω
Accuracy			±25		mV
Drift	0°C to 70°C		±50		ppm/°C
V_{REF} Input (Pins 18, P25):					Ω ‖ pF
Impedance[10]			363 ‖ 120		
POWER SUPPLY REJECTION	% of V_{OUT} / % of V_{SUPPLY}[11]		0.03		% / %
POWER SUPPLY REQUIREMENTS					
$\pm V_A$ Supply Voltage Range		±4.75	±5.00	±5.25	V
$+V_D$ Supply Voltage Range		+4.75	+5.00	+5.25	V
$+I_A$; $+I_D$ Combined Supply Current	$+V_A$; $+V_D$ = +5.0V		+28		mA
$-I_A$ Supply Current	$-V_A$ = –5.0V		–13		mA
Power Dissipation	$\pm V_A$ = ±5.0V; $+V_D$ = +5.0V		210	300	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) The PCM1750 is tested and guaranteed at 5.2µs, however it will operate at 4.5µs. The dynamic performance is not guaranteed or tested at this conversion rate. (3) Ratio of $Signal_{rms}$ / ($Distortion_{rms}$ + $Noise_{rms}$). (4) A/D converter sample frequency (4 x 48kHz; 4X oversampling per channel). (5) A/D converter input frequency (signal level). (6) Referred to input signal level. (7) Ratio of ($Distortion_{rms}$ + $Noise_{rms}$) / $Signal_{rms}$. (8) Externally adjustable to zero error. (9) Differential non-linearity error at bipolar major carry input code. Externally adjustable to zero error. (10) Full scale range (5.50V). (11) Refer to equivalent circuit in Figure 1. (12) Worst case operating condition. Refer to typical performance curves.

MECHANICAL

P Package — 28-Pin Plastic DIP

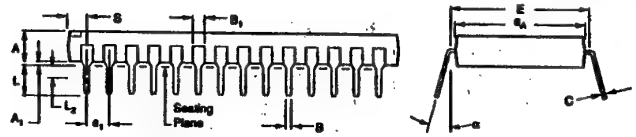


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A[1]	.160	.200	4.29	5.08
A1[1]	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.045	.055	0.38	1.40
C	.008	.012	0.20	0.30
D[1]	1.380	1.455	35.05	36.98
E	.600	.625	15.24	15.88
E1[1]	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

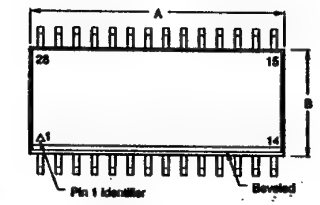
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	10°	0°	15°
θ[2]	.040	.060	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

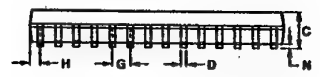


U Package — 28-Pin Plastic SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.700	.716	17.78	18.19
B	.296	.302	7.26	7.67
C	.093	.109	2.36	2.77
D	.016 BASIC		0.41 BASIC	
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.009	.012	0.20	0.30
L	.396	.414	10.11	10.52
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
1	–5V Analog Supply Voltage	$-V_A$
2	+5V Analog Supply Voltage	$+V_A$
3	Serial Output (Left Channel)	SOUTL
4	External Clock Input	CLK
5	+5V Analog Supply Voltage	$+V_A$
6	+5V Digital Voltage Supply	$+V_B$
7	+5V Digital Voltage Supply	$+V_B$
8	Digital Common Connection	DCOM
9	Analog Common Connection	ACOM
10	Digital Common Connection	DCOM
11	Convert Command Input	CONVERT
12	Serial Output (Right Channel)	SOUTR
13	+5V Analog Supply Voltage	$+V_A$
14	–5V Analog Supply Voltage	$-V_A$
15	Offset Adjust (Right Channel)	OFF_{ADJR}
16	MSB Adjust (Right Channel)	MSB_{ADJR}
17	Analog Voltage Input (Right Channel; ±2.75V)	V_{INR}
18	Reference Voltage Input (Right Channel)	$VREF_{INR}$
19	Reference Voltage Output (Right Channel)	$VREF_{OUTR}$
20	Analog Common Connection	ACOM
21	Reference Voltage Decouple	$VREF_{DEC}$
22	Reference Common Connection	RCOM
23	Analog Common Connection	ACOM
24	Reference Voltage Output (Left Channel)	$VREF_{OUTL}$
25	Reference Voltage Input (Left Channel)	$VREF_{INL}$
26	Analog Voltage Input (Left Channel; ±2.75V)	V_{INL}
27	MSB Adjust (Left Channel)	MSB_{ADJL}
28	Offset Adjust (Left Channel)	OFF_{ADJL}

ABSOLUTE MAXIMUM RATINGS

Analog Input Voltage (V_{IN})	$-V_A$ –0.3V to $+V_A$ + 0.3V
$+V_A$; $+V_B$ to ACOM/DCOM	0 to +7V
$-V_A$ to ACOM/DCOM	0 to –7V
$-V_A$ to $+V_A$; $+V_B$	0 to +14V
ACOM to DCOM	±1V
Digital Inputs (pins 4, 11) to DCOM	–0.3V to $+V_B$ + 0.3V
Power Dissipation	400mW
Lead Temperature, (soldering 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	80°C/W
Thermal Resistance, θ_{JA}: Plastic SOIC	100°C/W

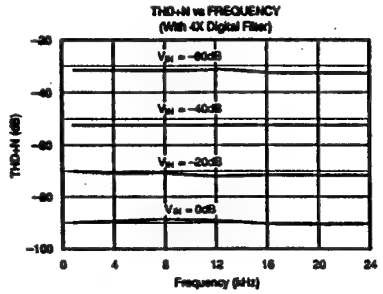
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

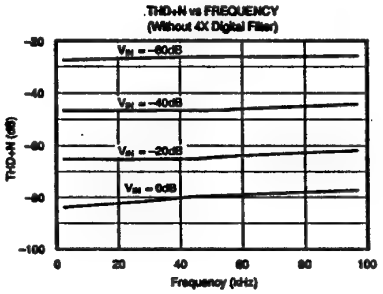
ORDERING INFORMATION

MODEL	PACKAGE
PCM1750P	Plastic DIP
PCM1750U	Plastic SOIC

TYPICAL PERFORMANCE CURVES

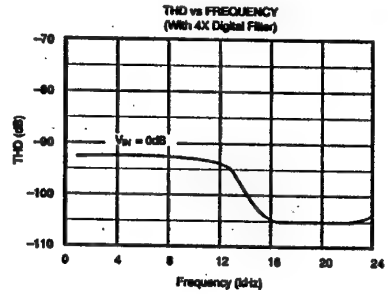
At 25°C, and $\pm V_A$ = ±5.0V; $+V_B$ = +5V, unless otherwise noted. Where relevant, specifications apply to both left and right input output channels.

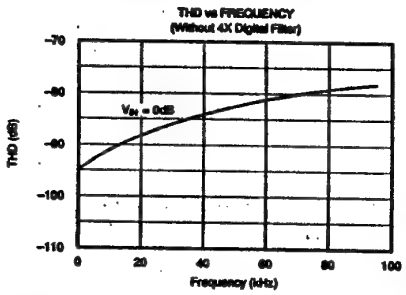


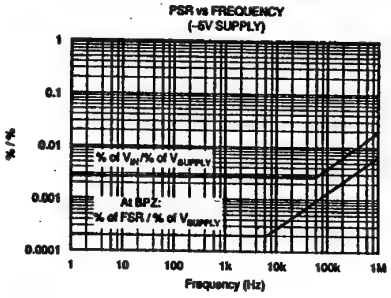


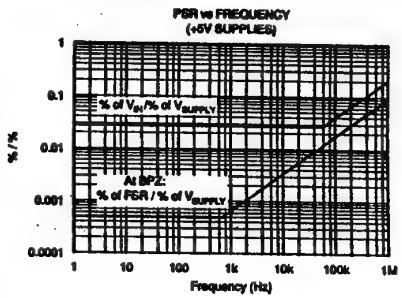
TYPICAL PERFORMANCE CURVES (CONT)

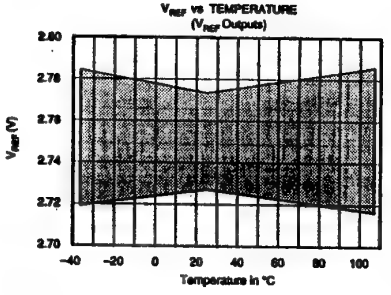
At 25°C, and $\pm V_A$ = ±5.0V; $+V_B$ = +5.0V, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.

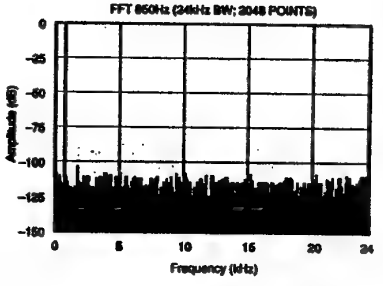






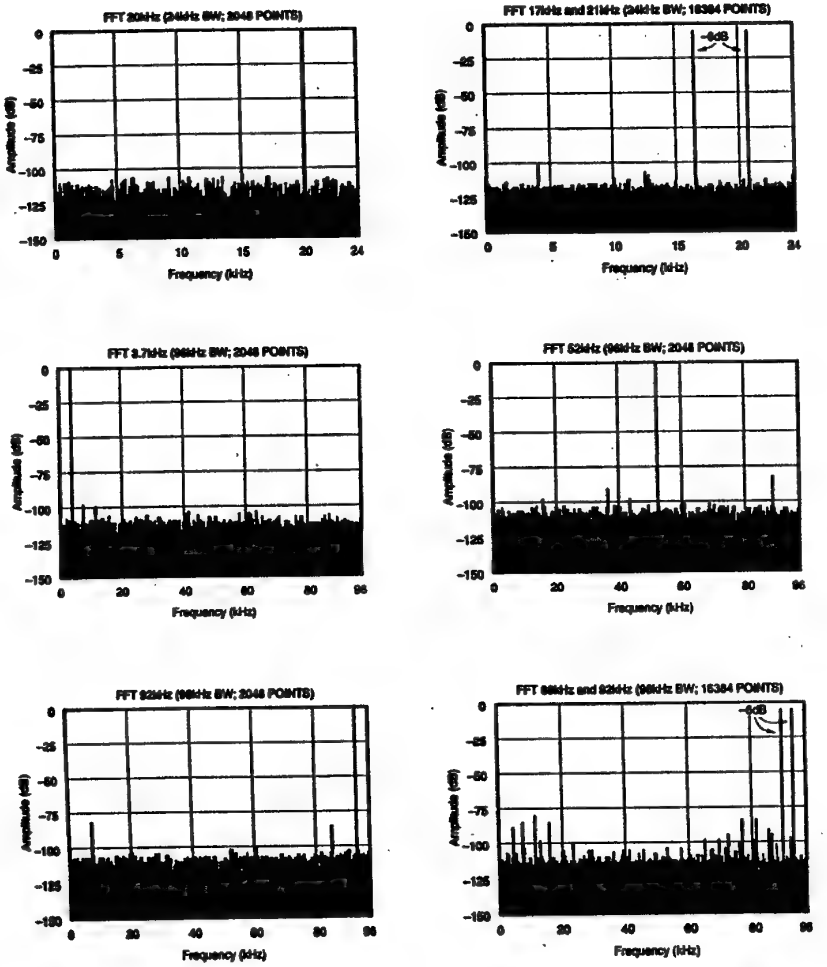






TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, and $\pm V_A$: $+V_S$ = ±5V, unless otherwise noted. Where relevant, specifications apply to both left and right input-output channels.



THEORY OF OPERATION

OVERVIEW

The PCM1750 is a dual 18-bit successive approximation CMOS analog-to-digital converter with serial data outputs designed especially for digital audio and similar applications. The single-chip converter is fabricated on a 3µ P-well CMOS process which includes poly-poly capacitors, laser-trimmable nichrome resistors, and two layers of interconnect metal. The dual converter employs a switched capacitor architecture which provides separate, simultaneous S/H (sample/hold) functions for each input channel. The separate S/H for each channel results in a desired feature called co-phase sampling which means that both S/H circuits are switched at the same time into the HOLD mode to capture their respective input signals simultaneously. This eliminates phasing errors produced by alternative architecture ADCs which do not sample the two input channels at the same time.

Switched binary-weighted poly-poly capacitors are used in CDAC (capacitive digital-to-analog converter) configurations to form the successive approximation converter sections

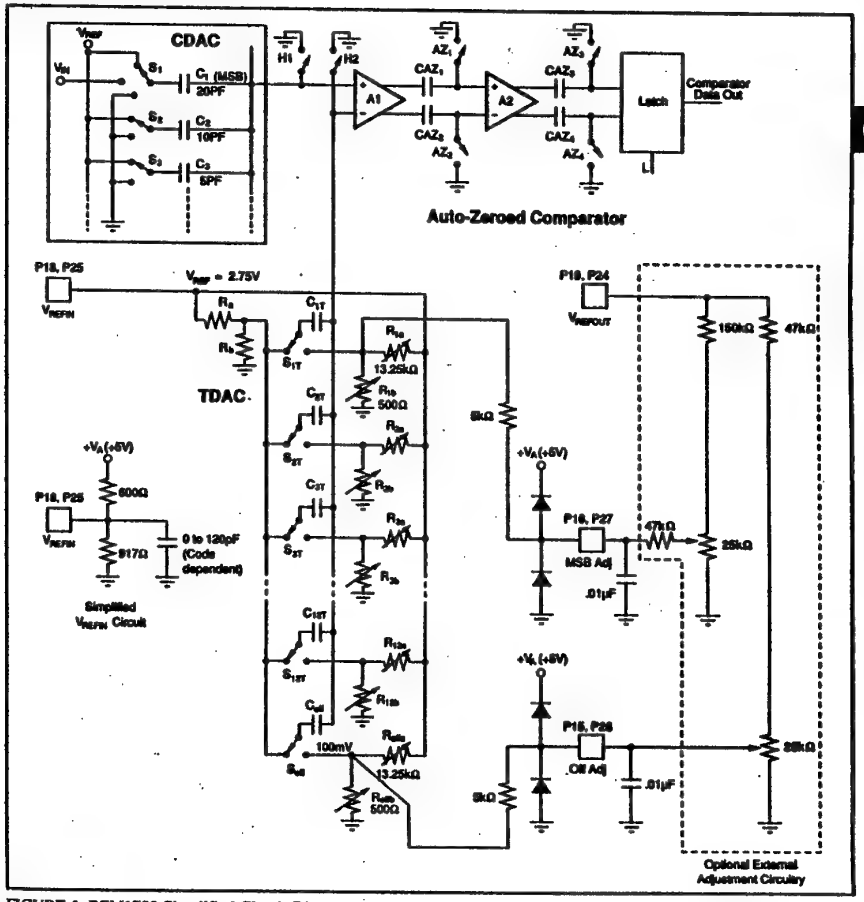


FIGURE 1. PCM1750 Simplified Circuit Diagram.

of the PCM1750. Two other switched-capacitor TDACs (trim-DACs, which employ laser-trimmed nichrome resistors) are also used to provide small correction voltages to the latching comparators. These small correction voltages compensate for ratio matching errors of the binary-weighted capacitors in the CDAC. The comparators contain autozeroed preamplifier stages ahead of the latching amplifier stage to produce a one bit, serial data stream that controls the successive approximation algorithm for each channel of the PCM1750.

To simplify user application, the PCM1750 includes an internal band-gap reference with fast settling buffer amplifiers to drive the CDACs. The dual converters operate synchronously (to minimize digital noise conversion errors) using an external system clock (normally at 1X, 2X or 4X the standard 48kHz audio sampling rate). By operating at a 2X or 4X over sampling rate the roll-off requirement for the input anti-aliasing filters is relaxed. For example, 1X systems typically use a 9 to 11 pole LPF (low pass filter) whereas a 4X system can use a 6th (or smaller) order filter when an appropriate digital filter such as the DF1750 is used in conjunction with the sampling system. Oversampling also has the added benefit of improved signal to noise ratio and total harmonic distortion. Two serial outputs, one for each input channel, provide binary-two's-complement coded output to an optional external digital decimation filter when over sampling operation is desired. The use of the optional companion digital filter, the DF1750, is described later in the installation and application sections of this product data sheet. A separate product data sheet is also available for the Burr-Brown DF1750 giving all the specifications and performance diagrams associated with this digital filter.

SAMPLE (TRACKING) MODE

After each conversion, the dual ADC returns to the SAMPLE mode in order to track the input signals. The switches shown in the simplified circuit diagram of Figure 1 will then be in the following states: S1 connects V_{IN} to C1 ; S2 to S18 connect C2 to C18 to V_{REF}; H1 and H2 connect the top plates of the capacitor arrays to analog common; and the latching comparator is switched into its auto-zero mode by closing AZ1 to AZ4. Notice that C1 serves two purposes: it samples and stores the input signal V_{IN} and it is the MSB of the CDAC. Storing V_{REF} on C2 to C18 creates a bipolar offset, enabling V_{IN} to cover a span from $-V_{REF}$ to $+V_{REF}$.

The 1/f noise as well as the DC input offset voltage of the comparator are removed by an autozeroing cycle which occurs during the SAMPLE period (see the timing diagram shown in Figure 2). These errors are stored on the AC coupling capacitors (CAZ1 to CAZ4, shown in Figure 1) between the gain stages. During the SAMPLE period the inputs to gain stages A1 and A2 and the latch are grounded by switches H1, H2, and AZ1 to AZ4. Capacitors CAZ1 and CAZ2 track the amplified offset voltage of gain stage A1 and capacitors CAZ3 and CAZ4 do the same for A2. At the beginning of a conversion cycle, the autozeroing switches open and the instantaneous amplified value of both the DC offset voltage and the low-frequency flicker noise is stored on the coupling capacitors to produce zero comparator offset during a conversion cycle.

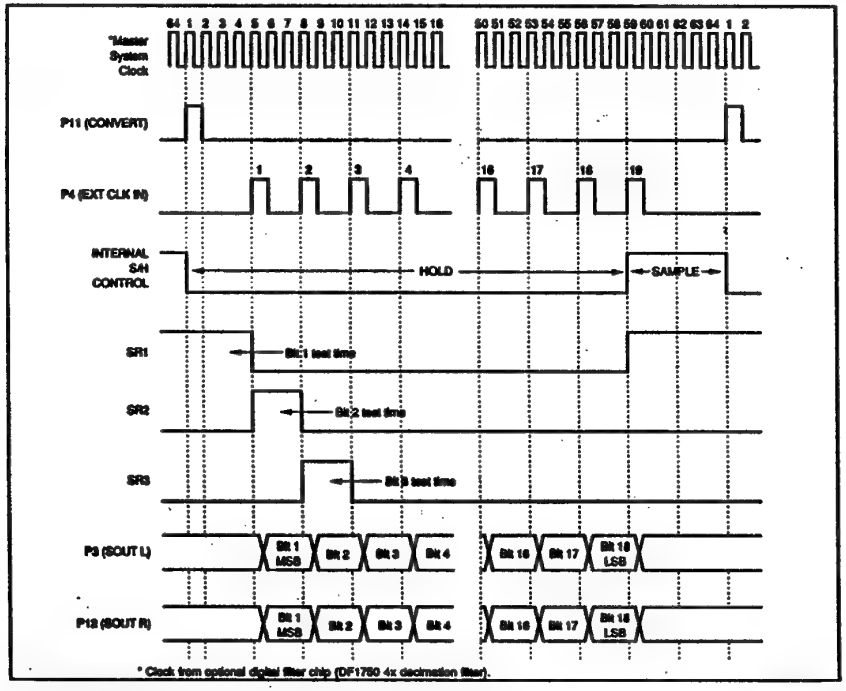


FIGURE 2. PCM1750 Input/Output Timing Diagram.

SUCCESSIVE APPROXIMATION CONVERSION PROCESS

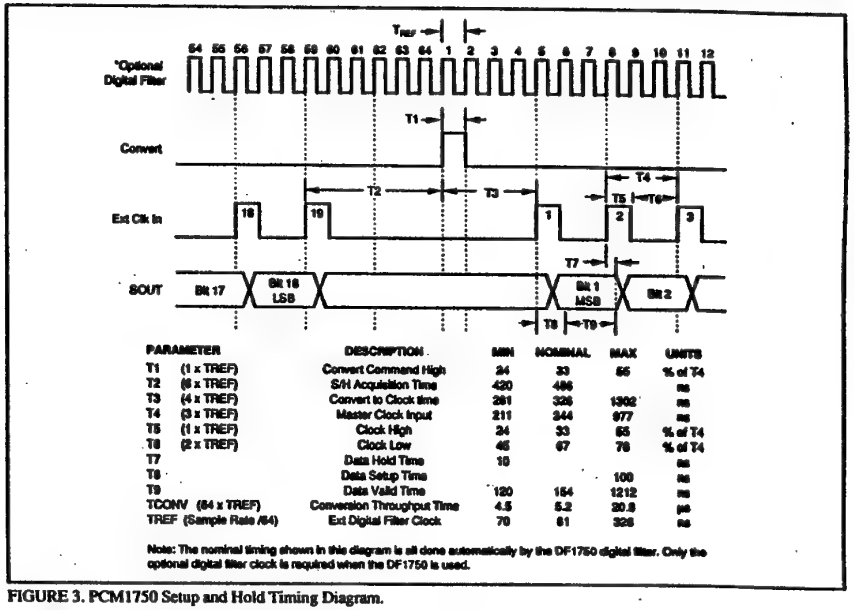
The timing diagram in Figure 2 illustrates the successive approximation routine of the PCM1750. Control signals CONVERT and CLK are derived from a master system clock which comes from a $256f_s$ (256 X the base sampling frequency of 48kHz) clock used by the optional digital filter. There are 64 clocks shown in the timing diagram because the PCM1750 is shown operating at 4 times the standard 48kHz sample rate (192kHz).

Several events occur on the rising edge of the CONVERT command. Switches AZ1 to AZ4, H1 and H2 open and switch S1 reconnects the MSB capacitor, C1, from V_{IN} to analog common (see Figure 1). This terminates the comparator auto-zero cycle and simultaneously switches (co-phase sampling) both converters from tracking their respective input signals into the HOLD mode, thus capturing the instantaneous value of V_{IN} (with a small delay specified as the aperture time).

At the start of a conversion cycle when S1 is switched to analog common, the sampled input signal V_{IN} will appear at the comparator input as $-V_{IN}/2$ due to the 2-to-1 capacitive divider action of C1 = C2 + C3 + ... C18. In a somewhat similar manner, V_{REF} is transferred to the comparator input as $-V_{REF}/2$ to create a bipolar offset.

The 19-bit shift register, shown in Figure 4, controls testing of the bits of the dual ADCs beginning with bit-1 (MSB) and proceeding one bit at a time to bit-18 (LSB), leaving ON those bits that don't cause the cumulative value of the CDAC to exceed the original input value and leaving OFF those bits that do. Since the bits of both channels are tested together, only one shift register is required to control both ranks of 18 data latches.

For example, the testing of bit-2 proceeds in the following manner. The positive pulse from the second shift register element SR2, (see Figure 2 and 4) is applied to the bit-2 data latch and NOR gate. The NOR gate in turn drives S2 and switches bit-2 at the beginning of the bit-2 test interval. Note that the bit interval must be long enough to allow both the comparator input to settle and the comparator to respond. On



PARAMETER		DESCRIPTION	MIN	NOMINAL	MAX	UNITS
T1	(1 x TREF)	Convert Command High	24	33	65	% of T4
T2	(6 x TREF)	S/H Acquisition Time	420	486		ns
T3	(4 x TREF)	Convert to Clock time	281	326	1302	ns
T4	(3 x TREF)	Master Clock Input	211	244	977	ns
T5	(1 x TREF)	Clock High	24	33	65	% of T4
T6	(2 x TREF)	Clock Low	46	67	76	% of T4
T7		Data Hold Time	10			ns
T8		Data Setup Time			100	ns
T9		Data Valid Time	120	154	1212	ns
TCONV	(64 x TREF)	Conversion Throughput Time	4.5	5.2	20.8	µs
TREF	(Sample Rate /64)	Ext Digital Filter Clock	70	81	326	ns

Note: The nominal timing shown in this diagram is all done automatically by the DF1750 digital filter. Only the optional digital filter clock is required when the DF1750 is used.

FIGURE 3. PCM1750 Setup and Hold Timing Diagram.

the next rising edge of CLKIN, at the end of the test interval, the comparator latch is strobed, providing a feedback logic level which tells the second data latch if bit-2 should be kept or rejected. This logic level is stored in the data latch and is passed on to switch S2 via the NOR gate on the falling edge of the pulse from SR2. This decision to keep or reject bit-2 moves the comparator input closer to a null condition, namely, zero potential. This sequential process continues for bit-3 through bit-18 and nulls the comparator inputs to within a value limited by the total system noise and the resolution/speed of the comparator.

Notice from the timing diagram in Figure 2 that the successive approximation algorithm operates synchronously with an external clock to minimize digitally-coupled switching noise from corrupting either the sample-to-hold operation or the critical comparator bit decisions. The two serial output data streams are derived synchronously from the respective latched comparator outputs and are available after a delay of one CLKIN cycle as illustrated in Figure 2. The serial output driver cells are TTL and CMOS compatible.

DIFFERENTIAL LINEARITY CALIBRATION

To understand the calibration of the PCM1750 it is necessary to discuss some of the characteristics of poly-poly capacitors. Poly capacitors are known to have equal or better stability and matching properties when compared to other precision components such as thin film resistors. On a well controlled process, ratio matching is typically 0.1%—a very respectable number for an untrimmed component. Even more impressive is their ratio tracking versus temperature of approximately 0.1ppm/°C.

Achieving DLE (differential linearity error) of less than 1/2 LSB at the 16-bit level requires ratio matching of the more significant bits to about 0.001%. Since the untrimmed ratio matching of poly capacitors is about two orders of magnitude larger than this requirement, a one-time factory calibration of the upper bits is required as described in the next section. Next, consider the effect of temperature due to the ratio tracking of 0.1ppm/°C. Over a 50°C span, DLE will change less than 1LSB at 18-bits; therefore, recalibration at temperature extremes is not necessary. Because of this excellent stability versus temperature (and versus time, also), the one-time factory calibration to correct initial DLE is more than satisfactory in meeting the accuracy requirements of the PCM1750.

TDAC OPERATION

Operation of the TDAC (trim DAC), which is laser trimmed at the wafer level, is described using bit-1 as an example. Switch S1T (see Figure 1) operates between two voltage levels—a reference level set by voltage divider Ra, Rb and a laser trimmable level set by R1a, R1b. The differences of these two levels is coupled by capacitor C1T to the minus input of the comparator to generate a correction voltage for

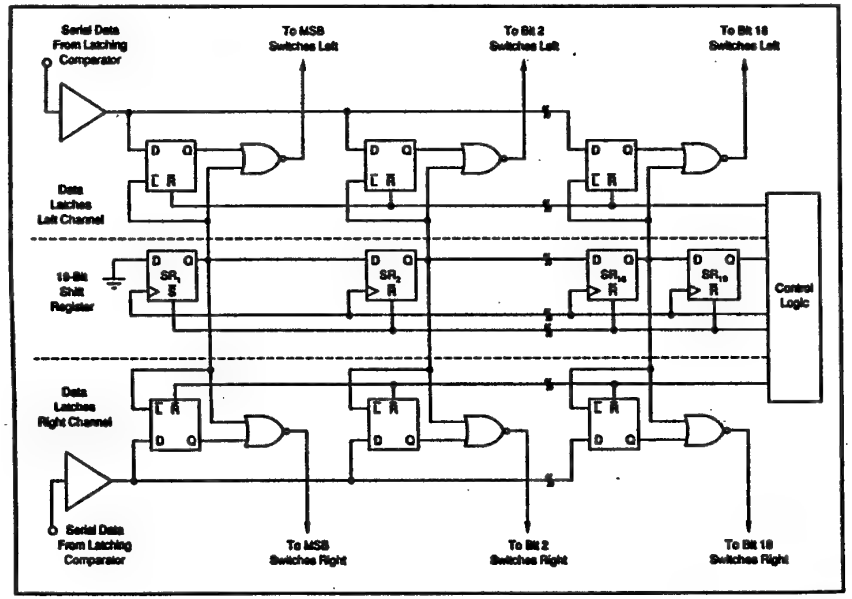


FIGURE 4. PCM1750 Successive Approximation Logic Diagram.

bit-1. The switches of the CDAC and the switches of the TDAC operate concurrently with each other, that is, when a decision is made to keep or reject bit-1, the same decision is made for the correction voltage for bit-1. Even though the ratio stability of the nichrome resistors used in the TDAC may not be as good as the poly capacitors, it is inconsequential because the correction voltage of each bit has a limited range of adjustment.

The DLE at the major carry (a code change from 111...111 to 000...000; in binary two's complement coding) is typically ±1/2 LSB at the 16-bit level, which is sufficient to provide 90dB SNR and –30dB low level distortion (–60dB input). For applications requiring less DLE at the major carry, a pin is provided for each channel to make an external MSB adjustment.

DISCUSSION OF SPECIFICATIONS

RESOLUTION AND DYNAMIC RANGE

The theoretical resolution of the PCM1750 is 18-bits. The maximum possible number of output codes or counts at 18-bits is 262,144 or 108dB (calculated by raising 2 to the 18th power). The relative accuracy of any A/D converter, however, is more a function of it's absolute linearity and signal-to-noise ratio than how many bits of resolution it has. These more pertinent specifications are described later in this section.

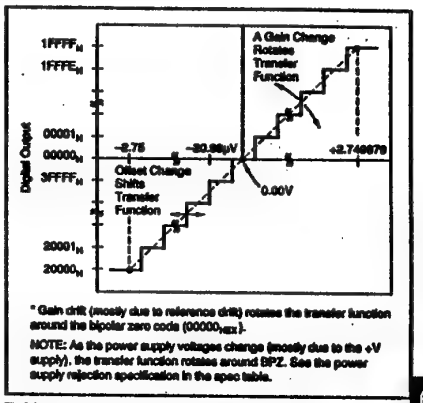
Dynamic range, as it is usually defined for digital audio converters, is the measure of THD + N at an effective input signal level of –60dB referred to 0dB. For the PCM1750 this value is typically 90dB and a minimum of 88dB (for audio bandwidth = 20Hz to 24kHz, THD + N at –60db = –30 db typ, –28dB max; f_{IN} = 1kHz and f_s = 192kHz). Resolution is also commonly used as a theoretical measure of dynamic range, but it does not take into account the effects of distortion and noise at low signal levels.

ANALOG INPUT RANGE

The analog input range for the PCM1750 is a bipolar ±2.75V (nominal). Table I gives the precise input/output and voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format. It should be noted that the computed voltage input levels represent center values (the midpoint between code transitions). Output coding is in binary two's complement.

DIGITAL OUTPUT	ANALOG INPUT	VOLTAGE INPUT
262144 LSBs	Full Scale Range	5.50000000V
1 LSB	Minimum Step Size	20.98083486nV
$1FFFF_{HEX}$	+Full Scale	+2.74997902V
00000_{HEX}	Bipolar Zero	0.00000000V
$3FFFF_{HEX}$	Bipolar Zero –1LSB	-0.00002098V
20000_{HEX}	–Full Scale	-2.75000000V

TABLE I. Analog Input to Digital Output Relationships.



* Gain drift (mostly due to reference drift) rotates the transfer function around the bipolar zero code (00000_{HEX}).

NOTE: As the power supply voltages change (mostly due to the +V supply), the transfer function rotates around BPZ. See the power supply rejection specification in the spec table.

FIGURE 5. Analog Input to Digital Output Diagram.

From Figure 5, the effects of offset and gain errors can be visualized. These errors can change value in response to changes in temperature and/or supply voltage. In addition, gain error (or the full scale range, FSR) changes in direct proportion to the $VREF_{IN}$ voltage value.

SAMPLE AND HOLD PARAMETERS

Aperture Delay and Uncertainty

Aperture delay is the time required to switch from the SAMPLE to HOLD mode. This time is typically 10ns for the PCM1750 and it is constant. Aperture uncertainty (jitter) is the amount of uncertainty associated with the aperture delay. Aperture uncertainty affects the overall accuracy of the converter and is greatest at the maximum input frequency of the converter. The formula for determining the maximum input frequency (f_{MAX}) for a given error contribution due to aperture uncertainty is: $f_{MAX} = (2 \times \pi \times t_{rms} \times 2^N)^{-1}$ where t_{rms} is the RMS aperture uncertainty and 2^N is the desired SNR (signal-to-noise ratio) expressed in total number of quantization levels. A 15-bit SNR, therefore, would be expressed as 2^{15} or 32768. Using the typical PCM1750 aperture jitter of $50ps_{rms}$ and an SNR at the 15-bit level, $f_{MAX} = (2 \times \pi \times 50ps \times 32768)^{-1}$ or 97.1kHz. This matches very closely with the rated dynamic accuracy of the PCM1750 where THD + N = –88dB max. This means the typical aperture jitter of PCM1750 only becomes a factor when input signals to it exceed 97kHz and/or an SNR greater than 15-bits is desired.

Input Bandwidth

The full power bandwidth of the PCM1750 is that input frequency above which significant distortion is observed (THD+N > 10-bits or –60dB for a full scale input signal). In the data sheet, this number is specified as typically being 500kHz. In wideband operation (when no digital filter is used) the additional full power bandwidth of the PCM1750

can be used to purposely alias a band-limited signal down into the baseband of the converter. This technique is called undersampling and can be used to directly down-convert an intermediate frequency riding on a much higher carrier frequency.

DIGITAL I/O AND TIMING

Input/Output Logic Compatibility

Digital logic on the PCM1750 is CMOS compatible. Digital outputs on the PCM1750 are capable of driving a minimum of two standard TTL input loads.

Digital output coding is in binary two's complement. Table I gives the precise input/output voltage/code relationships for the PCM1750. Figure 5 shows these same relationships in a graphical format.

Convert Command and External Clock Input

A conversion is initiated on its positive going edge of the convert command. Although the convert command can return low at any time (prior to 50ns before the rising edge of the 19th clock), a typical convert command pulse width of 81ns (as called out in Figure 3) is specified for a 192kHz sample rate (f_S). The reason for a pulse width spec is to reduce problems associated with digital logic feedthrough noise. The return of convert command to a logic low level in the specified time interferes least with the successive approximation process. Also, it should be noted that putting fast logic edges (<5ns) on convert command (P11) and the external clock input (P4) may cause logic feedthrough to the analog stages in the converter and will result in added distortion during the sampling and conversion process. Using the optional DF1750 digital filter provides adequately slow transitions to maintain full specification performance. If necessary, an external RC, on the convert command line may be used to slow fast logic edges.

As with the convert command, the external clock input is positive edge triggered and is not duty-cycle dependent other than to improve digital feedthrough noise immunity. A 50% duty cycle clock can be used instead of 33% if desired. Refer to Figure 3 for recommended timing relationships. Regardless of what clock duty cycle is used, all operations relating to valid data clocking should be synchronized to the rising edge of the clock input.

Although there is a maximum conversion time called out in the specification table, the PCM1750 can have a considerably longer conversion cycle. Droop of the internal capacitors will ultimately determine what the true maximum conversion time can be. The min/typ/max times shown in Figure 3 are based on minimum sample rate of 48 kHz, a typical of 192kHz, and a maximum of 222kHz. All specifications are tested at 192kHz. The minimum sample rate assumption is based on clock periods that increase as time between convert commands increases. Any sample rate down to near DC can be utilized by observing maximum clock cycle requirements and spacing convert commands to achieve lower sample rates. This means that the time interval T2 shown in Figure 3 does not have a maximum value.

Clock Lockout

Any number of clocks can be given to the PCM1750 beyond the 19 required for normal operation. If a continuous clock is used, all clocks beyond the 19th are gated off by the PCM1750's internal logic until the next positive going edge of the convert command. The converter also goes into the sample (track) mode starting on the positive edge of the 19th clock until the next positive edge of the convert command, regardless of how many additional clocks are offered. The ideal operation of the converter stops the clock input after the 19th during this critical signal acquisition time. This is the timing shown in Figure 3 . The critical timing aspect that must be observed if a clock input other than the recommended is used, is that ample time following the positive edge of convert command proceed the next rising clock edge. If this time is shortened, the most important bit-1 (MSB) decision, which is finalized on the first clock edge after convert command, will be adversely affected. In other words, the clock input cannot have a rising edge during the time interval T3 shown in Figure 3.

SIGNAL-TO-NOISE RATIO

Another specification for A/D converters is signal-to-noise ratio (SNR). For this measurement, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz. An FFT is performed on the digital output and the noise power in the non-harmonic audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

One advantage of using the PCM1750 in this oversampled mode with the optional DF1750 digital decimation filter is that the converter noise is spread over the full 0Hz to 96kHz passband and then suppressed by the digital filter stopband attenuation (from 24kHz to 96kHz). This effectively increases the SNR of the PCM1750 by 6dB when it is used as an audio bandwidth converter. The other advantage is that the need for a higher-order anti-aliasing input filtering is greatly reduced.

THD + N

The key specification for the PCM1750 is total harmonic distortion plus noise (THD + N). In terms of signal measurement, THD + N is the ratio of $Distortion_{RMS} + Noise_{RMS}$ / $Signal_{RMS}$ expressed in dB. For the PCM1750, THD + N is 100% tested at all three specified input levels using the production test setup shown in Figure 6. For this measurement, as with the SNR test, a full-scale 1kHz signal is applied and the sampling rate of the PCM1750 is set at 192kHz (which is 4X the standard digital audio sample rate of 48kHz). An FFT is performed on the digital output and the total power in all audio-bandwidth frequency bins (20Hz to 24kHz) is summed and expressed in relation to the full-scale input signal.

For the audio band, the THD+N of the PCM1750 is essentially flat for all frequencies and input signal levels. In the *Typical Performance Curves* THD + N versus Frequency plots are shown at four different input signal levels (with and without a 4X decimation filter): 0dB, –20dB, –40dB, and –60dB.

CHANNEL SEPARATION

To test channel separation a 1kHz signal sampled at 192kHz is placed on one input of the PCM1750 while the other input is held at 0V. An FFT is performed on the idle (0V) channel and the result checked to insure that the 1kHz tone is suppressed by a minimum of 96dB.

GAIN AND OFFSET ERRORS

Initial gain and bipolar offset errors are laser trimmed at the wafer level and 100% final tested to insure compliance with the electrical specifications. Bipolar offset errors can be further reduced to zero by using the optional offset adjustment circuitry shown in the connection diagram (Figure 7). Gain errors can be adjusted by varying V_{REF} to either channel of the converter. This is accomplished by either using an adjustable external reference or by placing buffer amplifiers with adjustable gain between $VREF_{OUT}$ and $VREF_{IN}$ as shown in Figure 8a.

INTEGRAL AND DIFFERENTIAL LINEARITY

DC Linearity Testing

The absolute linearity of the PCM1750 is on the order of 15-bits or more as can be seen from the THD versus Frequency plots in the *Typical Performance Curves*. Not every code in the converter must be 15-bit linear to achieve the specified THD + N performance, but a very high percentage will be that linear. The same observation also applies to differential linearity errors in the PCM1750. Because the PCM1750 is not 100% tested for DC linearity specifications, no minimum or maximum specifications are given for integral or differential linearity errors.

No Missing Codes Operation

A no missing codes specification is not given for the PCM1750 for the same reasons as given above. The PCM1750, however, typically has fewer than 16 codes (less than 0.01%) missing at a 14-bit resolution level. A 100% no missing codes specification cannot be maintained above the 12-bit level, although this has very little impact on overall dynamic performance (THD + N). The few missing codes that do occur at higher resolution levels are at the bit-2 and lower major carry transitions of the converter. There are typically no missing codes (at 14-bits) around the critical bipolar zero operation zone (±1/8 of full scale range around bipolar zero or 0V). The critical bipolar differential linearity error can be reduced from its initial value to zero using the optional MSB adjustment circuitry shown in the connection diagram (Figure 7).

REFERENCE

The gain drift of the PCM1750 is primarily due to the drift associated with the reference. Better drift performance can be achieved using an external reference like the ones explained in the applications section (Figures 8b, 8c). The *Typical Performance Curves* plot of V_{REF} Output versus Temperature shows the full range of operation including initial error and typical gain drift. Pertinent performance data are found in the electrical specification table.

Reference Bypass

Both P18 and P25 ($VREF_{IN}$) should be bypassed with a 10µF to 47µF tantalum capacitor. If there are important system reasons for using the PCM1750 reference externally, the outputs of P19 and P24 must be appropriately buffered, and bypassed (see Figure 8).

POWER SUPPLY REJECTION

Because of the architecture of the PCM1750, power supply rejection varies with input signal size. The spec table value is expressed in the relative terms of percent of V_{IN} per

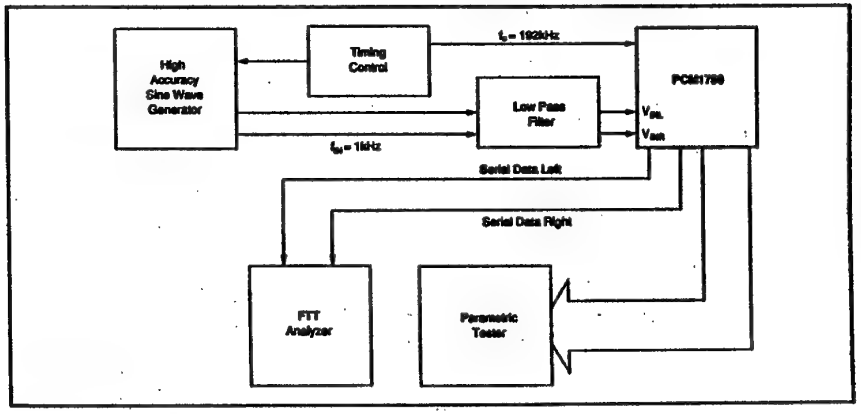


FIGURE 6. PCM1750 Production Test Setup.

percent change of the supply voltage. The PSR versus Frequency plot in the *Typical Performance Curves* show PSR expressed versus an increase in power supply ripple frequency.

PERFORMANCE OVER TEMPERATURE

Specification Temperatures

All critical specifications are tested at 25°C. The drift specification temperature range is from 0°C to +70°C. The PCM1750 will operate over the wider temperature range of -40°C to +85°C.

Gain and Offset Drift

Although the PCM1750 is primarily meant for use in dynamic applications, specifications are also given for more traditional DC drift parameters such as temperature gain and offset drift. The primary cause of drift in the PCM1750 is the bandgap reference. Much lower gain drift can be realized if necessary by using any circuit similar to the external reference circuits shown in Figure 8. Also, refer to the *Typical Performance Curves* of V_{REF} Output versus Temperture.

Dynamic Performance

Dynamic performance is predominated by the absolute linearity of the PCM1750. Because of the excellent ratio tracking versus temperature of poly-poly capacitors, there is virtually no change in dynamic performance of the converter over temperature (primarily THD + N). The dynamic specifications over temperature cannot be guaranteed, however, as they are not 100% tested.

INSTALLATION

ANTI-ALIASING FILTER

To prevent unwanted input signals from being aliased into the passband of the converter, it is necessary to suppress all out of band signals above 1/2 the sampling frequency of the ADC by using a low-pass filter. The requirement for an anti-aliasing filter, however, can be reduced by using oversampling techniques. By raising the sample rate of the converter by a factor of 2 or even 4, the roll off of the anti-aliasing filter can be reduced. In Figure 9, a 6th order, linear-phase, anti-aliasing filter is implemented using low-cost dual audio op amps. This filter will suppress frequencies above 96kHz by 80dB. For many applications a 4th or 2nd order anti-aliasing filter will be adequate when using the PCM1750 in the 4X oversampling mode.

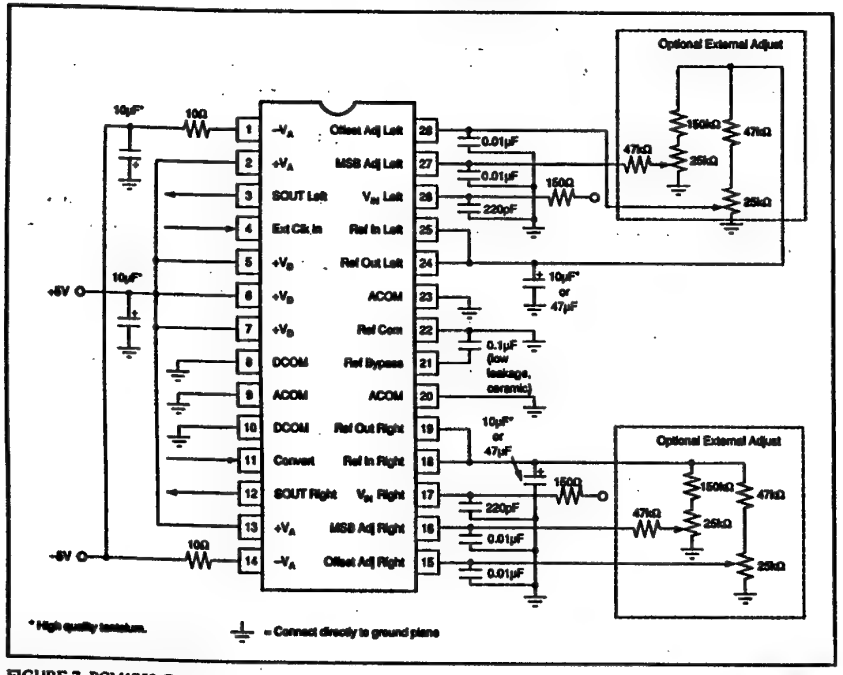


FIGURE 7. PCM1750 Connection Diagram.

INPUT SIGNAL CONDITIONING

RC Input Circuit

Note the 150Ω resistors and 220pF capacitors on each analog input as shown in the connection diagram (Figure 7). This input circuit configuration is required to achieve optimum SNR performance of the PCM1750. Various other component values will yield satisfactory results, but the resistor should never exceed 200Ω.

Buffer Amplifier

To avoid introducing distortion, the PCM1750 input must be driven by a low active impedance source (op amps such as the NE5532, Burr-Brown OPA2604, or equivalent are ideal).

EXTERNAL ADJUSTMENTS

The simplified circuit diagram (see Figure 1) shows one of two complete channels on the PCM1750. The input switched capacitors, trim DAC and comparator are detailed. The trim DAC switches are activated whenever the corresponding bit is chosen during the successive approximation routine. The first 12 bits of the ADC have corresponding trim DAC circuits. The R1a to R12a and R1b to R12b resistors can be laser trimmed at the wafer level if necessary to correct for any nonlinearities. The nominal voltage for the internally generated V_{REF} is 2.75V and it is a relatively low impedance, buffered voltage output. It should be noted that just the act of connecting the optional adjustment circuits will affect the MSB DLEs and bipolar offsets since it is unlikely that the initial potentiometer settings (even if centered) would match the factory trimmed null potentials. If connected, the potentiometers must be properly adjusted.

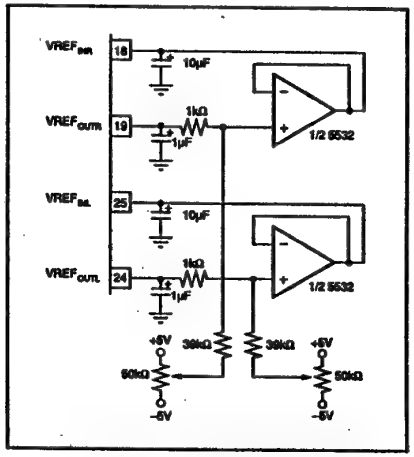


FIGURE 8a. Circuit for External Gain Adjustment Using the Internal Reference.

MSB Adjust

The MSB adjust pin connects to the center of the R1a/R1b resistive divider for bit-1. After laser trimming this point is nominally 100mV. All the MSB and offset adjust pins should be connected to ground using a 0.01µF capacitor, especially if traces to the potentiometers are long. If the adjust pins are not used, they should still be bypassed to ground.

Since there are internal 5kΩ resistors and clamp diodes to both ground and +5V on the MSB and offset adjust pins, there are obvious limits to their range of adjustment. With a nominal internal voltage on these points of +100mV, there will be a greater limitation in making negative adjustments than positive. A negative voltage at either adjustment pin, however, is acceptable up to one diode drop (-0.6V) below ground.

The preferred method of MSB DLE adjustment is to input a small level signal and adjust for minimum THD + N.

Offset Adjust

The offset adjust switch (S_{OFF}) position is controlled by whether the ADC is in the sample or hold mode. Switching from sample to hold effectively allows any charge offsets associated with the sampling process to be eliminated. Grounding the input to the converter as far ahead of the A/D as possible (in front of the anti-aliasing filter for example) and then adjusting the bipolar zero error will remove the offsets associated with the entire sampling system.

LAYOUT CONSIDERATIONS

Power Requirements

Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used. Although the PCM1750 positive supplies have separate digital and analog +5V, for most applications the +5V digital supply pins should be connected to the +5V analog supply. If they aren't connected together, a potential latchup condition can occur when the power supplies are not turned on at the same time. If one supply pin is powered and the other is not, the PCM1750 may latch up and draw excessive current. In normal operation, this is not a problem because both $+V_A$ and $+V_D$ should be connected together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "hot" socket exists, care should be taken to power the PCM1750 only after it has been socketed.

All supplies should be bypassed as shown in Figure 7. The bypass capacitors should placed as close to their respective supply pins as possible. Additional .01µF capacitors may be placed in parallel with the larger value capacitors to increase high-frequency rejection, but generally they are not required when high quality tantalums are used. The 0.1µF capacitor between P21 and P22 should be a low leakage type (such as ceramic) and must be put as close to these pins as possible to reduce noise pickup.

The PCM1750 is sensitive to supply voltages outside the absolute maximum ratings shown in the specification tables. Do not exceed –8V on the negative supplies at any time or irreversible damage may occur. Note the 10Ω resistors in series with each –5V supply line (shown in Figure–7) to help protect the part from severe damage if the supplies are over-ranged momentarily.

Grounding Requirements

Because of the high resolution and linearity of the PCM1750, system design problems such as ground path resistance and contact resistance become very important.

The ACOM and DCOM pins are separated internally on the PCM1750. To eliminate unwanted ground loops, all commons (both analog and digital) should be connected to the same low-impedance ground plane. This should be an analog ground plane separate from other high-frequency digital ground planes on the same board. If the analog and digital commons of the PCM1750 are connected to different ground planes, care should be taken to keep them within 0.6V of each other to insure proper operation of the converter.

A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signals should be referenced to the ACOM pins. This will prevent voltage drops in the power supply returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external MSB and offset adjust potentiometers are used, the potentiometers and related resistors should be located as close to the PCM1750 as possible.

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. Care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the PCM1750 has an internal sample/hold function, the signal that switches it into the HOLD state (CONVERT going HIGH) is critical, as it would be on any sample/hold amplifier. The CONVERT rising edge should have minimal ringing, especially during the 20ns after it rises.

APPLICATIONS

USING A DIGITAL FILTER

A 4X decimation filter is available for the PCM1750 called the DF1750. It is available in a 28-pin DIP or a 40-pin SOIC package. The use of this filter greatly eases the implementation of the PCM1750 in audio band applications.

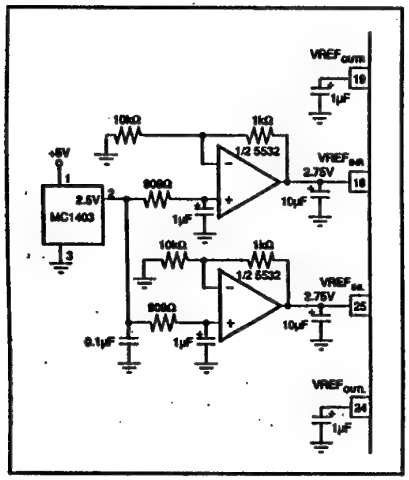


FIGURE 8b. External Reference Circuit Using Standard 2.5V Reference.

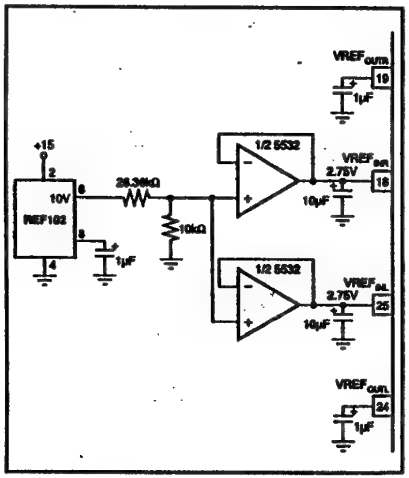


FIGURE 8c. Low Noise, Low Drift External Reference Circuit.

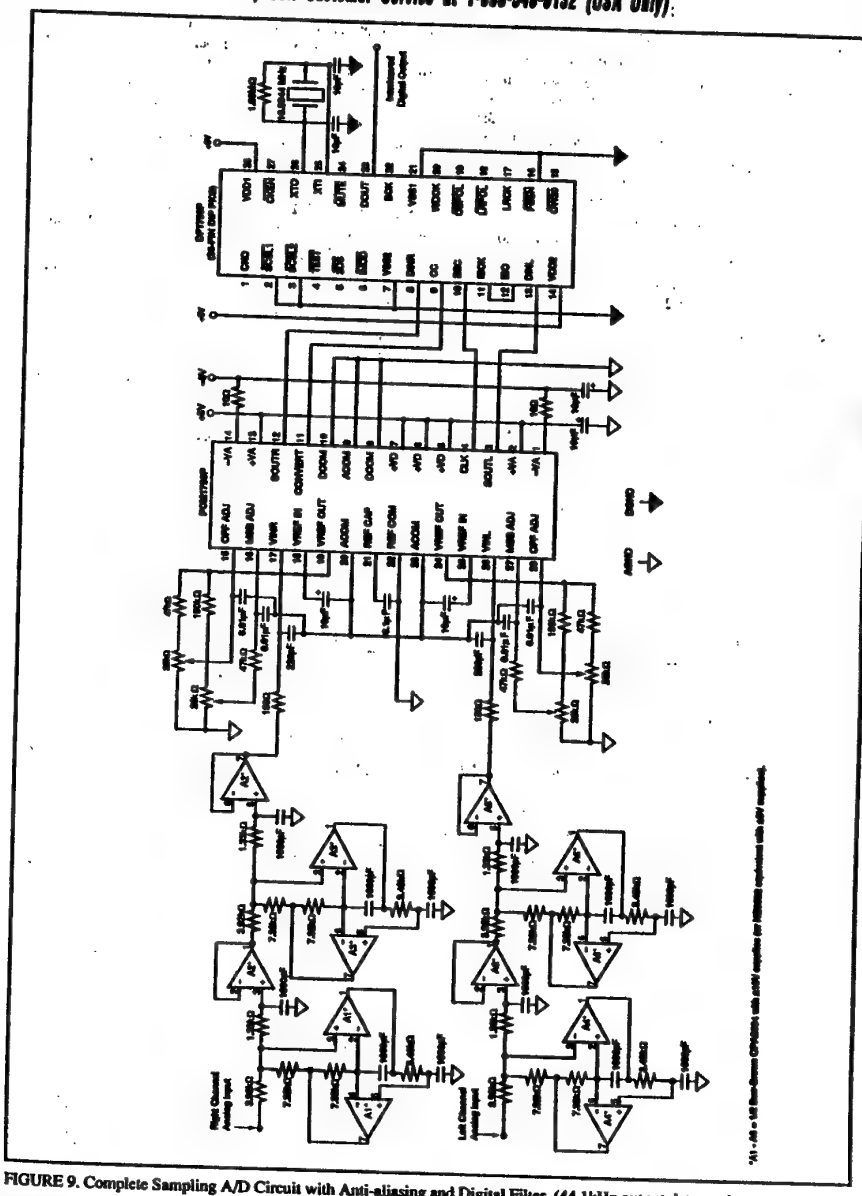


FIGURE 9. Complete Sampling A/D Circuit with Anti-aliasing and Digital Filter, (44.1kHz output data rate).

USING AN EXTERNAL REFERENCE

Normally $VREF_{OUT}$ is connected directly to $VREF_{IN}$. The typical value for V_{REF} versus Temperature is shown in the *Typical Performance Curves*. If better drift or power supply rejection performance is desired, one of the external reference circuits shown in Figures 8b and 8c can be used. Note that the decoupling capacitors are still connected to $VREF_{IN}$. External gain adjustment is now possible by using the variable output options available on some precision voltage references or by varying the gain on external buffer amplifiers. The range of acceptable external references is from +2.0V to $+V_A$ – 2.0V, with 2.5V types being the most commonly available. Full scale input voltage range will be $\pm VREF_{IN}$ (a +2.5V $VREF_{IN}$ results in a ±2.5V input range).

If an external reference is used, P19 and P24 must be bypassed with at least 1µF capacitors.

SAMPLING A/D SYSTEM

Figure 9 is a partial schematic of the demonstration fixture for the PCM1750 (orderable by model number DEM1133). It shows the implementation of (1) a 6th order, linear-phase, anti-aliasing filter (22kHz low-pass); (2) the PCM1750P A/D converter; and (3) a 4X digital decimation filter called the DF1750P. Not shown on this schematic, but included on the demo fixture, are latched parallel data outputs with strobe and a serial digital interface format (SPDIF) data transmitter. Also included on the DEM1133 are user breadboard areas for application specific circuit implementation.

CONNECTION TO DSP WITH DIGITAL FILTER

The PCM1750 and DF1750 combination can be connected to the serial ports of most popular DSP processor ICs (such as those made by AT&T, Motorola, TI, and AD) by adding a small amount of external glue logic. Figures 10 and 11 show the timing diagram and schematic for this interface.

To use this interface, the DSP processor IC must be configured for 32 bit word inputs. The glue logic generates a flag bit, as the first bit of the 32 bit word, that signifies either left or right channel data. The flag bit will be low for left channel data and high for right channel data.

The DF1750 can be configured for either 16 or 20 bit data, although only 16 bit data is shown in Figure 10. After the data is transferred into the DSP processor IC, it must be shifted toward the LSB by one bit in order to compensate for a clock delay in the glue logic.

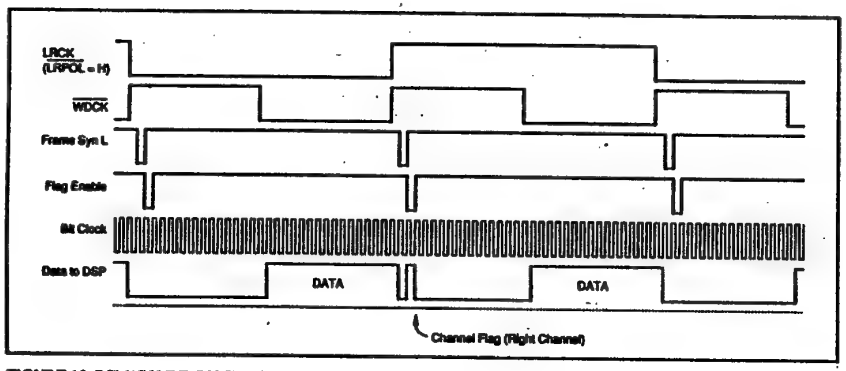


FIGURE 10. PCM1750/DF1750 To DSP IC Timing Diagram.

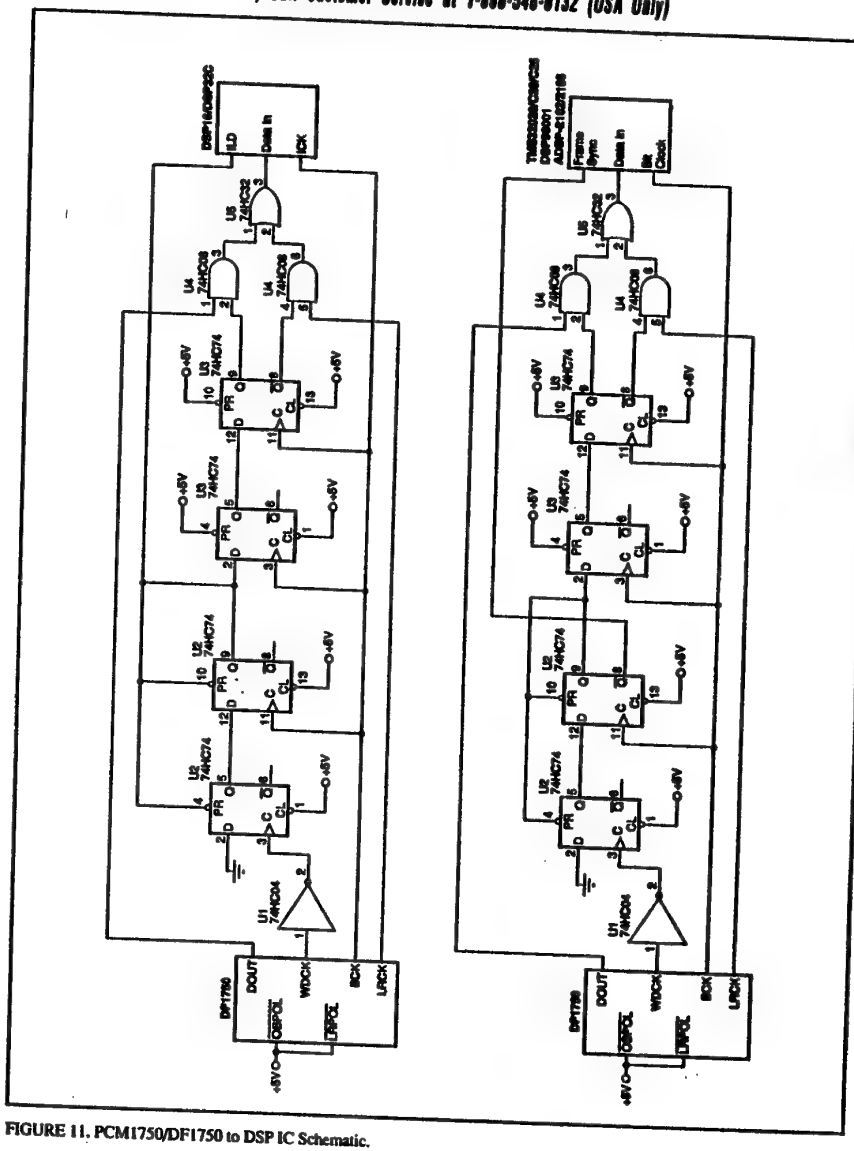


FIGURE 11. PCM1750/DF1750 to DSP IC Schematic.

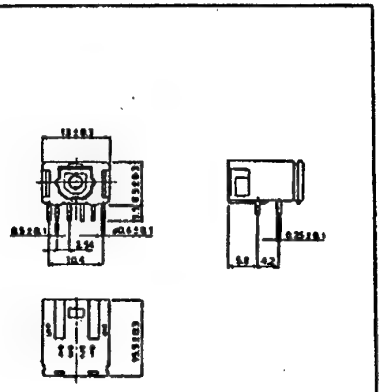
TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

Fiber Optic Transmitting Module
TOTX195

Fiber Optic Transmitting Module for Simplex Digital signal transmission.

- Data rate : DC to 10 M b/s(NRZ code).
- Transmission distance : Up to 50 m.
- TTL interface.
- LED is driven by Differential circuit.

Unit: mm



1 GND
2 Current limitting resistor of LED.
3 Vcc
4 Input
5 Non Connection.
6 Non Connection.

TEKELEC AIRTRONIC
5, rue Carle Vernet
92315 SEVRES CEDEX
FRANCE
Yannick BAILLY
Tél. : 33 (1) 46 23 24 25
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Télex : 269 746 sous adresse
116 8746 - TEKELEC

1. Absolute Maximum Ratings. (Ta=25℃)

Item	Symbol	Rating	Unit
Storage Temperature	T_{STG}	-40 to 85	℃
Operating Temperature	T_{OPR}	-40 to 85	℃
Supply Voltage	V_{CC}	-0.5 to 7	V
Input Voltage	V_{IN}	-0.5 to Vcc+0.5	V
Soldering Temperature	T_{SOL}	260 (1)	℃

Note (1) Soldering time≦ 3 seconds.

TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

TOTX195

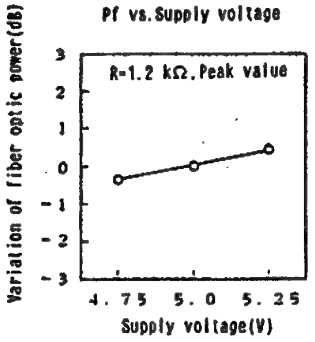
2. Electrical and Optical Characteristics. (Ta=25℃, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	unit.
Data Rate		NRZ Code (2)	DC	-	10	Mb/s
Transmission Distance		Using APF (3) and TORX194	-	-	50	m
Delay Time(L→H) (4)	t_{PLH}	Using APF and TORX194	-	-	120	ns
Delay Time(H→L) (4)	t_{PHL}	Using APF and TORX194	-	-	120	ns
Pulse Width Distortion (4)	Δt_W	Using APF and TORX194 Pulse width 100 ns Repetition 200ns, CL=10pF	-30	-	30	ns
Fiber Output Power	P_f	APF 2m, R=1.2kΩ (5)	-11	-	- 6	dBm
Peak Emission Wavelength	λ_P		-	670	-	nm
Current Consumption	I_{CC}	R= 1.2kΩ	-	35	55	mA
High Level Input Voltage	V_{IH}		2.0	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Input Current	I_{IH}		-	-	20	μA
Low Level Input Current	I_{IL}		-	-	-0.4	mA

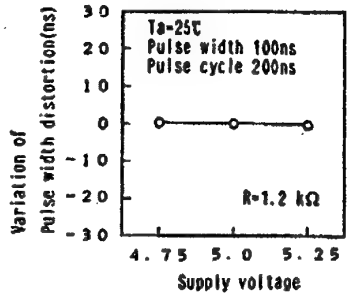
(2) LED is on when input signal is high level, it is off when low level.
(3) All Plastic Fiber(980/1000μm) with polished surface.
(4) Between input of TOTX195 and output of TORX194.
(5) Measure with a standard optical fiber with fiber optic connectors. Valued by peak.

Example of Typical Characteristics

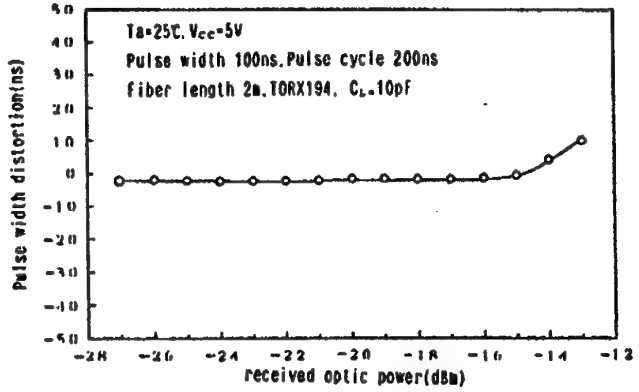
Pf vs. Supply voltage



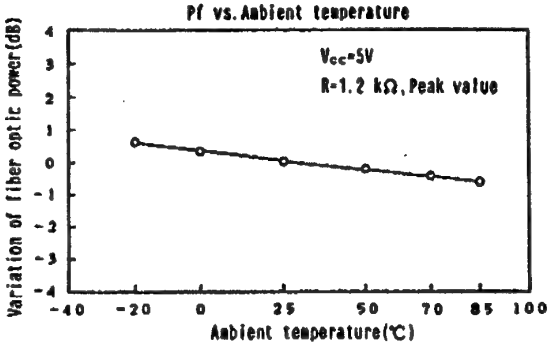
Δtw vs. Supply voltage



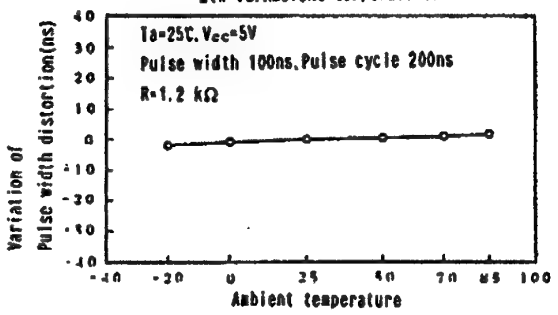
Pulse width distortion vs. Received optic power



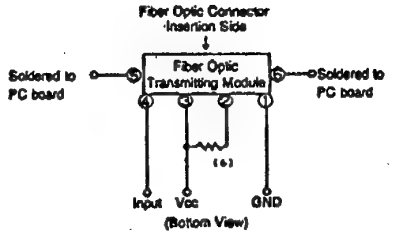
Pf vs. Ambient temperature



Δtw vs. Ambient temperature.



3. Connection Method



Note(4) Select a resistor value as follows:

Transmission Distance (m)	Resistor (Ω)
0.2 to 10	17.8 k
10 to 30	6.2 k
30 to 50	1.2 k

4. Applicable optical fiber with fiber optic connectors.

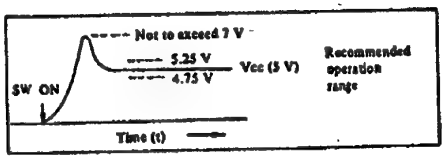
TOCP100-**HB, TOCP155-**HB, TOCP100P-**HB, TOCP155P-**HB.

5. Precautions for operation.

(1) The absolute maximum ratings shows the limits, which must not be exceeded even momentarily regardless of the external condition.
Operation beyond the limit of the absolute maximum ratings may cause failure of the device.

(2) Please be sure to solder Pins No. 5 and NO.6 of TOTX195 to PC board.

(3) Power supply voltage.



(4) Do not use acid or alkaline soldering fulx cleaner solvent.
Please be careful not inject the solvent into module through the fiber optic connector holl.
If some solvent happens to be injected into the module, wipe off with a cotton boll. The recommended cleaner solvent is thichrolethane.

(5) When not using the module, always provide an attached protective cap to it.

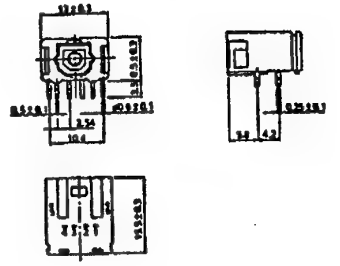
OSHIBA SEMICONDUCTOR
TECHNICAL DATA

Fiber Optic Receiving Module
TORX194

Unit mm

Fiber Optic Receiving Module for Simplex Digital signal transmission.

- Data rate : DC to 10 M b/s(NRZ code).
- Transmission distance
  : Up to 50 m(APF).
  : Up to 1000 m(PCF).
- TTL Interface.
- ATC(Automatic Threshold Control) Circuit is used for stabilized output at a wide range of optical power level.



1	Output
2	GND 1
3	Vcc
4	GND 2
5	Case
6	Case

TEKELEC AIRTRONIC
5, rue Carle Vernet
92315 SEVRES CEDEX
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Télex : 269 746 sous adresse
HG 8746 TEKELEC

1. Absolute Maximum Ratings(Ta=25 ℃)

Item	Symbol	Rating	Unit
Strage Temperature	T_{STG}	-40 to 85	℃
Operating Temperature	T_{OPR}	-40 to 85	℃
Supply Voltage	V_{CC}	-0.5 to 7	V
Low Level Output Current	I_{OL}	20	mA
High Level Output Current	I_{OH}	-1	mA
Soldering Temperature	T_{SOL}	260 (1)	℃

Note (1) Soldering time ≦ 3 seconds.

TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

TORX194

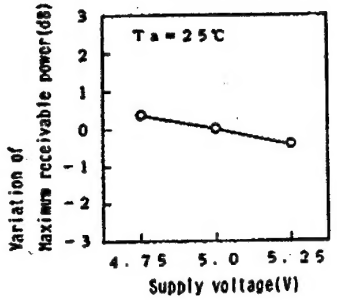
2. Electrical and Optical Characteristics (Ta=25℃, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Date Rate		NRZ code (2)	DC	-	10	Mb/s
Transmission Distance		Using APF (3), TOTX195	0.2	-	50	m
		Using PCF (4), TOTX194	0.2	-	1000	m
Delay Time(L→H)	t_{PLH}	Fiber length 2m.	-	-	120	ns
Delay Time(H→L)	t_{PHL}	Fiber length 2m.	-	-	120	ns
Pulse Width Distortion (5)	Δt_W	Pulse width 100ns Pulse cycle 200ns C_L=10pF	-30	-	30	ns
Maximum Receivable Power (6)	P_{MAX}	10Mb/s, APF, TOTX195	-14	-	-	dBm
		10Mb/s, PCF, TOTX194	-18	-	-	dBm
Minimum Receivable Power (6)	P_{MIN}	10Mb/s, APF, TOTX195	-	-	-27	dBm
		10Mb/s, PCF, TOTX194	-	-	-29	dBm
Current Consumption	I_{CC}		-	22	40	mA
High Level Output Voltage	V_{OH}		2.7	-	-	V
Low Level Output Voltage	V_{OL}		-	-	0.4	V

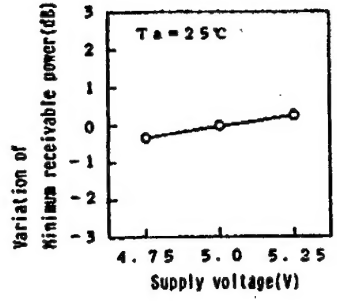
Note (2) The duty factor must be such as kept 25 to 75 %.
High level output when optical flux is received. Low level output when optical flux is not received.
(3) All Plastic Fiber (980/1000 μm) with polished surface.
(4) Plastic clad silica fiber (200/300μm) with polished surface.
(5) Between input of a fiber optic transmission module and output of TORX194.
(6) BER ≦ 10^{-9}, valued by peak.

Example of Typical Characteristics

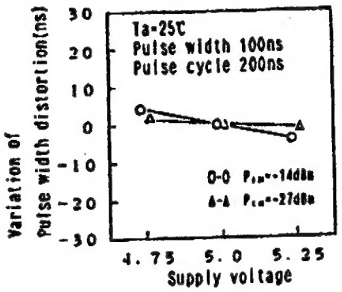
$P_{MAX.}$ vs. Supply voltage



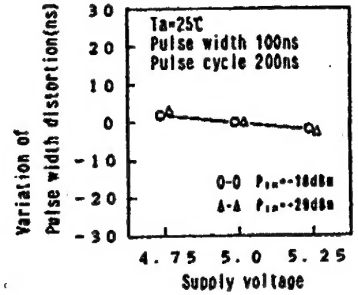
$P_{MIN.}$ vs. Supply voltage



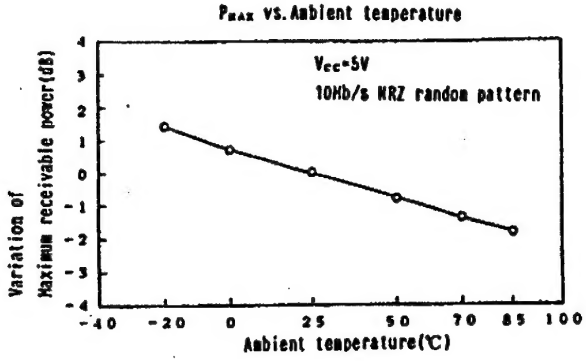
Δtw vs. Supply voltage (APF)



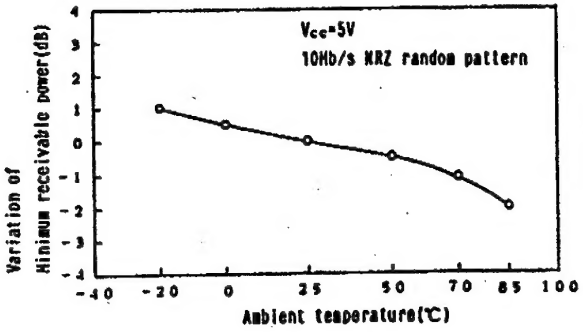
Δtw vs. Supply voltage (PCF)



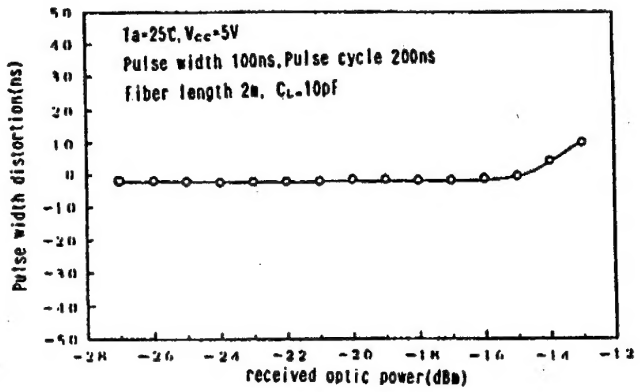
P_{MAX} vs. Ambient temperature



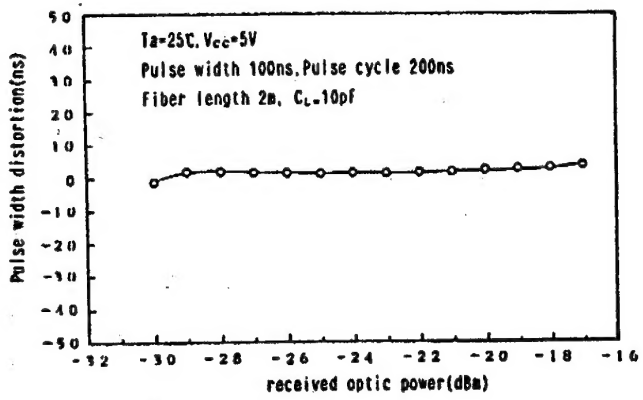
$P_{MIN.}$ vs. Ambient temperature



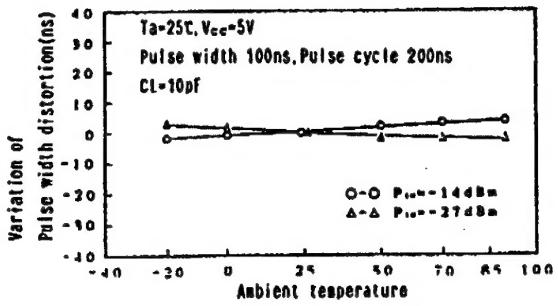
Pulse width distortion vs. Received optic power (APF)



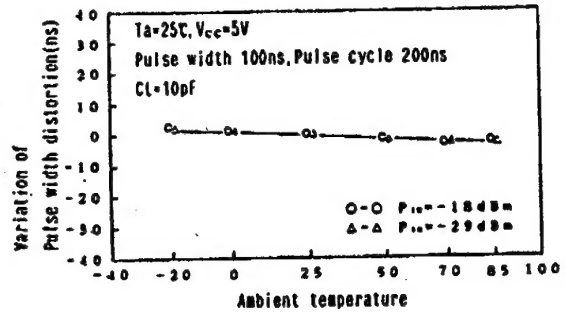
Pulse width distortion vs. Received optic power (PCF)



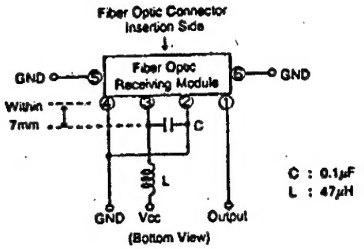
Atw vs. Ambient temperature. (APF)



Atw vs. Ambient temperature. (PCF)



3. Connection Method



4. Applicable optic conncal fiber with fiber optic connectors.

TOCP100-••HB, TOCP155-••HB, TOCP100P-••HB, TOCP155P-••HB(APF).
TOCP100Q-••HB, TOCP150Q-••HB, TOCP101Q-••HB, TOCP151Q-••HB, TOCP156Q-••HB
TOCP100X-••HB, TOCP150X-••HB, TOCP101X-••HB, TOCP151X-••HB, TOCP156X-••HB(PCF).

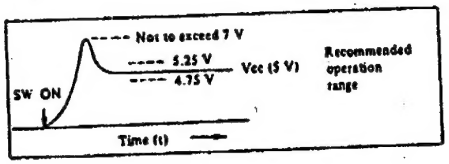
5. Precautions for operation

(1) The absolute maximum ratings show the limits, which must not be exceeded even momentarily regardless of the external condition.
Operation beyond the limit of the absolute maximum rating may cause failure of the device.

(2) Pins No.5 and No.6 of TORX194 are ground pins of housing. The housing is made of conductive plastic for shielding purpose.
Please be sure to ground these pins for efficient shielding.

(3) Additional precaution is necessary to ensure that conductive housing dose not touch other potential patterns.

(4) Power supply voltage



(5) Do not use acid or alkaline soldering flux cleaner solvent.
Please be careful not inject the solvent into module through the fiber optic connector hole.
If some solvent happens to be injected into the module, wipe it off with a cotton ball. The recommended cleaner solvent is thichrolethane.

(6) When not using the module, always provide an attached protective cap to it.

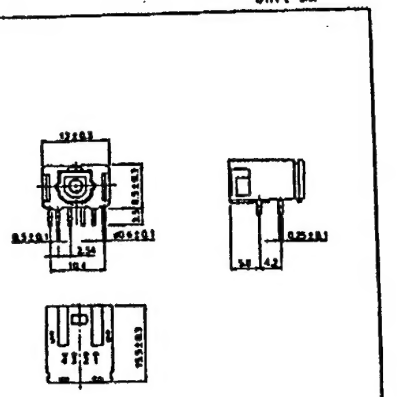
TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

Fiber Optic Receiving Module
TORX194

Unit mm

Fiber Optic Receiving Module for Simplex Digital signal transmission.

- Data rate : DC to 10 M b/s(NRZ code).
- Transmission distance
  : Up to 50 m(APF).
  : Up to 1000 m(PCF).
- TTL Interface.
- AIC(Automatic Threshold Control) Circuit is used for stabilized output at a wide range of optical power level.



1	Output
2	GND 1
3	Vcc
4	GND 2
5	Case
6	Case

1. Absolute Maximum Ratings(Ta=25 ℃)

Item	Symbol	Rating	Unit
Strage Temperature	T_{STG}	-40 to 85	℃
Operating Temperature	T_{OPR}	-40 to 85	℃
Supply Voltage	V_{CC}	-0.5 to 7	V
Low Level Output Current	I_{OL}	20	mA
High Level Output Current	I_{OH}	-1	mA
Soldering Temperature	T_{SOL}	260 (1)	℃

Note (1) Soldering time ≦ 3 seconds.

TOSHIBA SEMICONDUCTOR
TECHNICAL DATA

TORX194

2. Electrical and Optical Characteristics (Ta=25℃, Vcc=5V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Date Date		NRZ code (2)	DC	-	10	Mb/s
Transmission Distance		Using APF (3), TOTX195	0.2	-	50	m
		Using PCF (4), TOTX194	0.2	-	1000	m
Delay Time(L→H)	t_{PLH}	Fiber length 2m.	-	-	120	ns
Delay Time(H→L)	t_{PHL}	Fiber length 2m.	-	-	120	ns
Pulse Width Distortion (5)	Δt_W	Pulse width 100ns Pulse cycle 200ns C_L=10pF	-30	-	30	ns
Maximum Receivable Power (6)	P_{MAX}	10Mb/s, APF, TOTX195	-14	-	-	dBm
		10Mb/s, PCF, TOTX194	-18	-	-	dBm
Minimum Receivable Power (6)	P_{MIN}	10Mb/s, APF, TOTX195	-	-	-27	dBm
		10Mb/s, PCF, TOTX194	-	-	-29	dBm
Current Consumption	I_{CC}		-	22	40	mA
High Level Output Voltage	V_{OH}		2.7	-	-	V
Low Level Output Voltage	V_{OL}		-	-	0.4	V

Note (2) The duty factor must be such as kept 25 to 75 %.
High level output when optical flux is received. Low level output when optical flux is not received.
(3) All Plastic Fiber (980/1000 μm) with polished surface.
(4) Plastic clad silica fiber (200/300μm) with polished surface.
(5) Between input of a fiber optic transmission module and output of TORX194.
(6) BER ≦ 10^{-9}, valued by peak.